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# MS-7817

mATX

Ver: 10

## Intel Sharkbay plamform H81

CPU:

INTEL-Haswell LGA1150

System Chipset:

INTEL-LYNX

Memory:

DDRIII (1333/1666MHz) \* 2 (Dual Channel)

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:RTL892

LAN-realtek8111G

SIO:NUVOTON 5533D

SPI ROM: 64 MB

Other:

DVI\*1

VGA\*1

SATA2\*2

SATA3\*2

FRONT USB2.0 \*2

REAL USB2.0 \*4

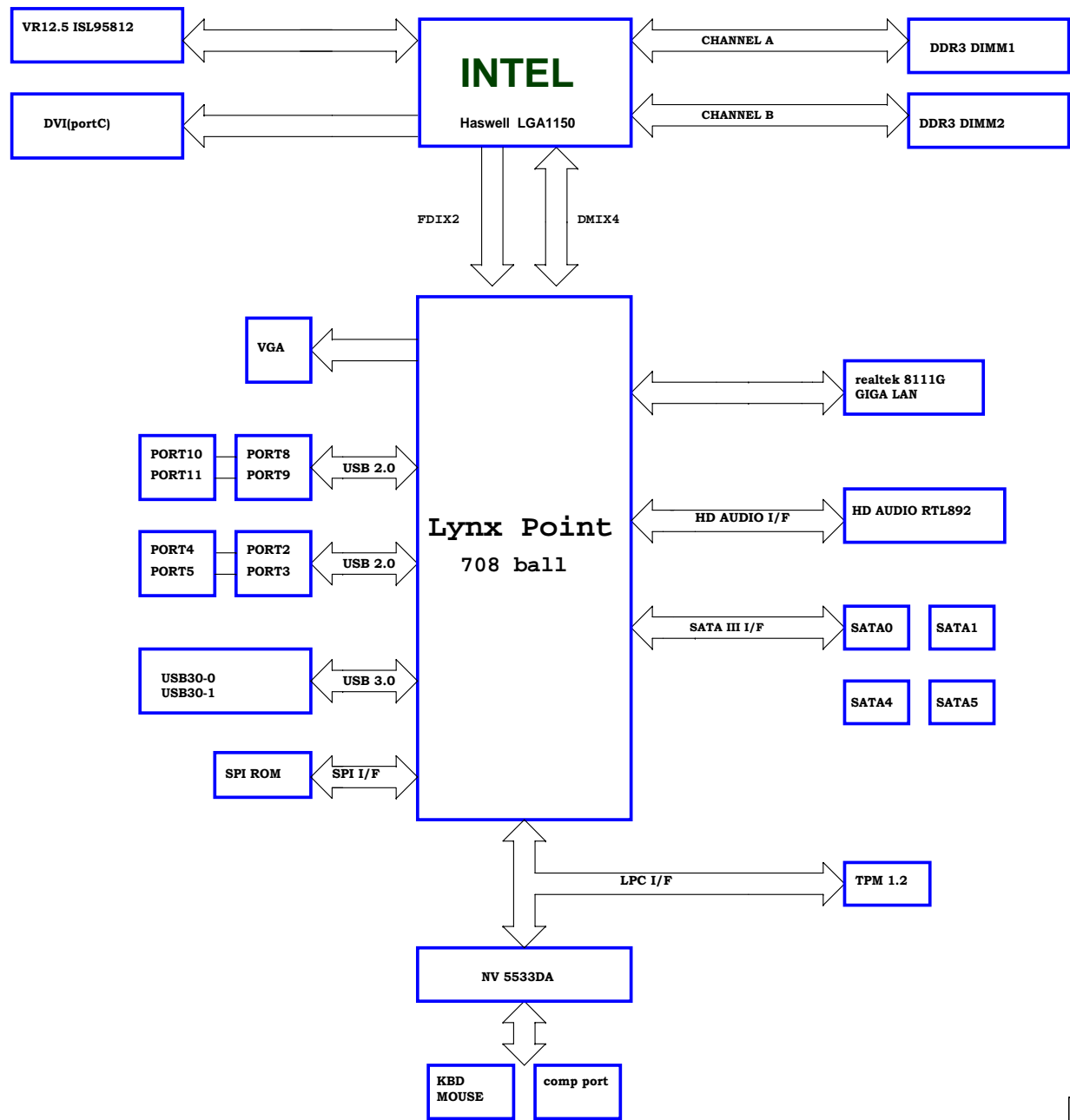
REAL USB3.0 \*2

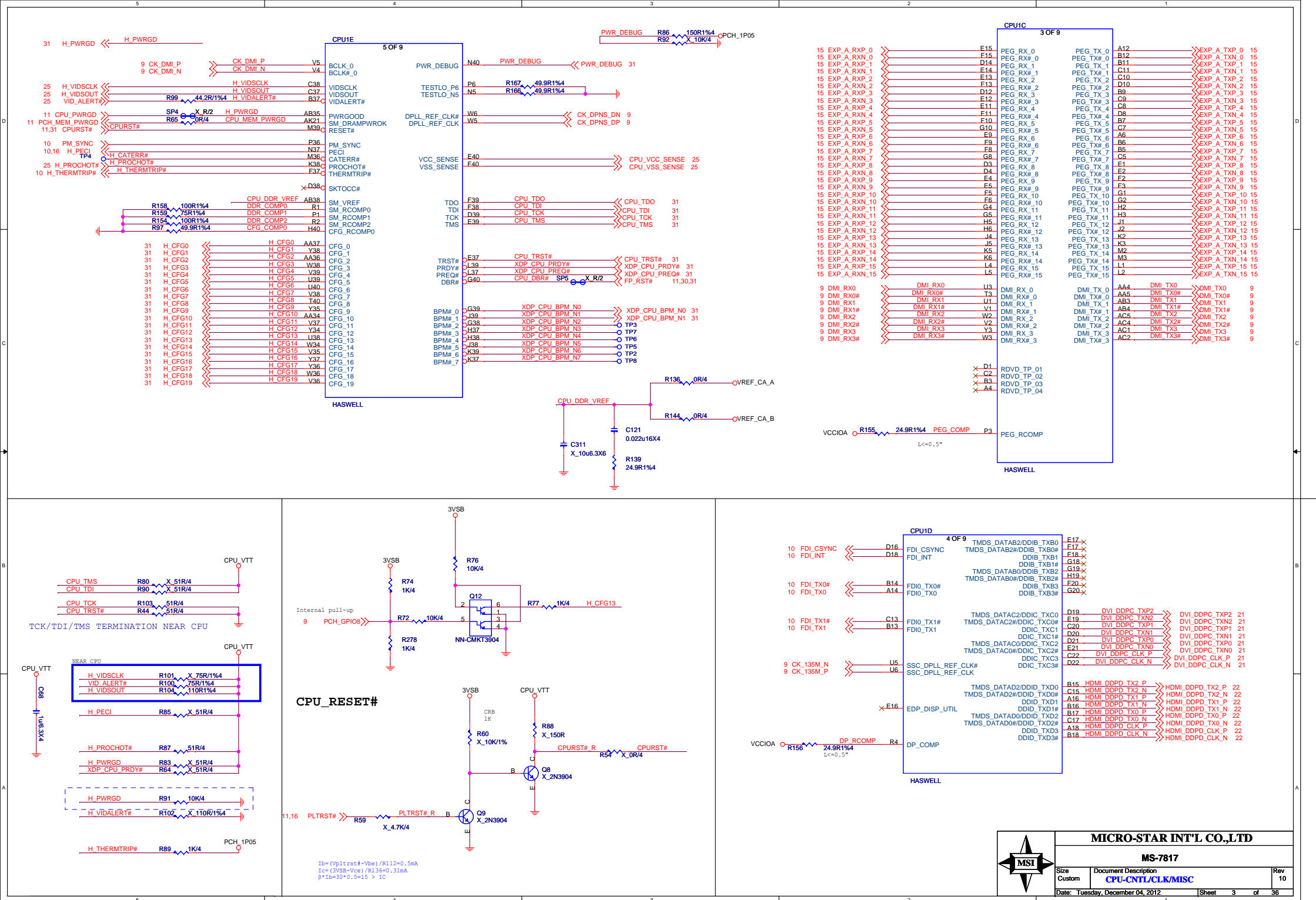
Expansion Slots:

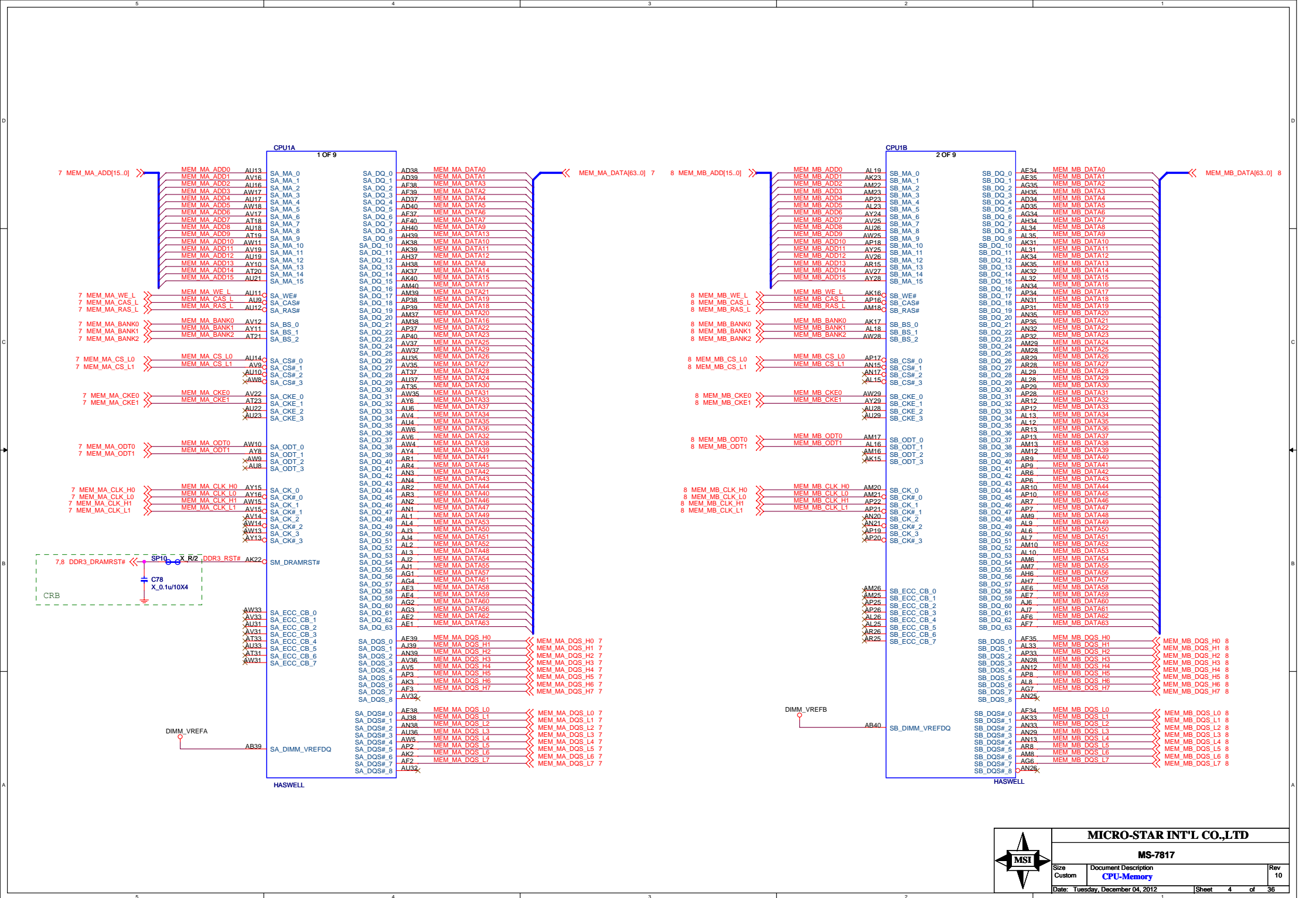
PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 1

MS-7817 Block Diagram







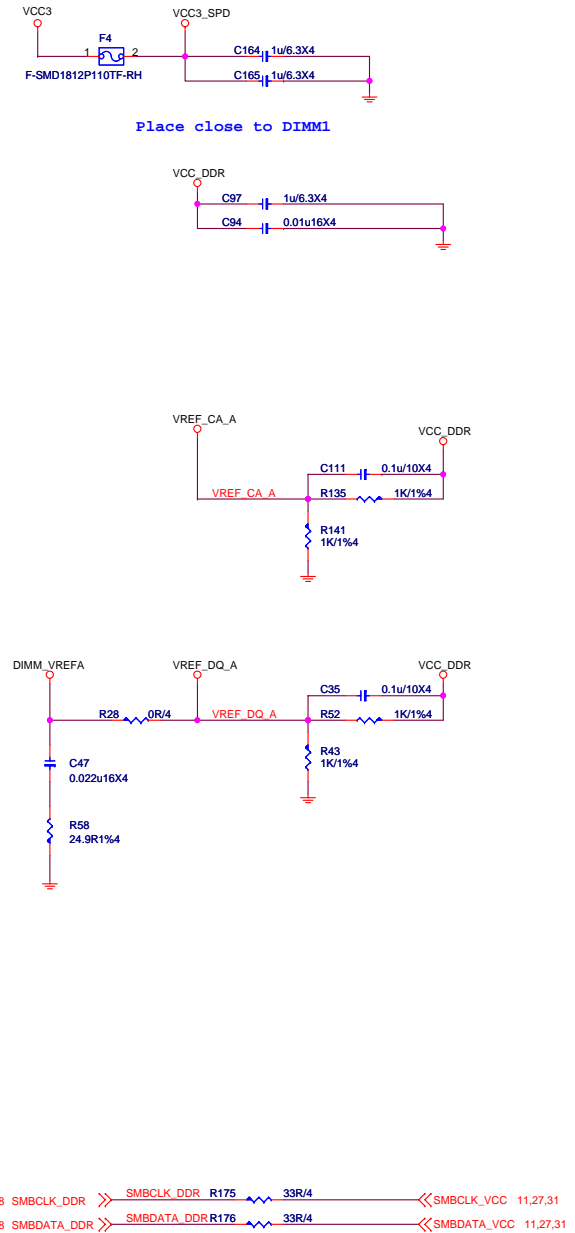
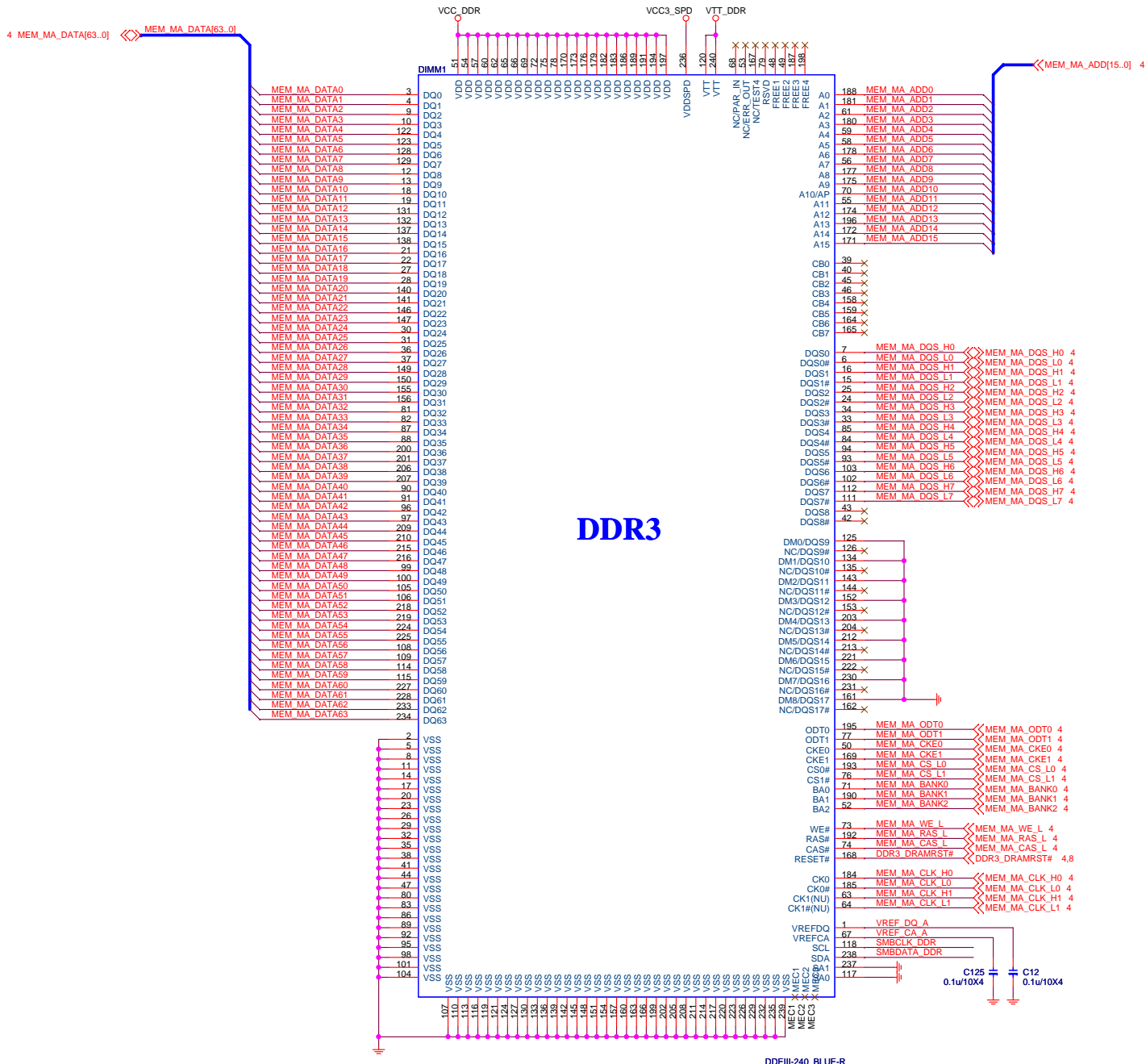


GND

GND

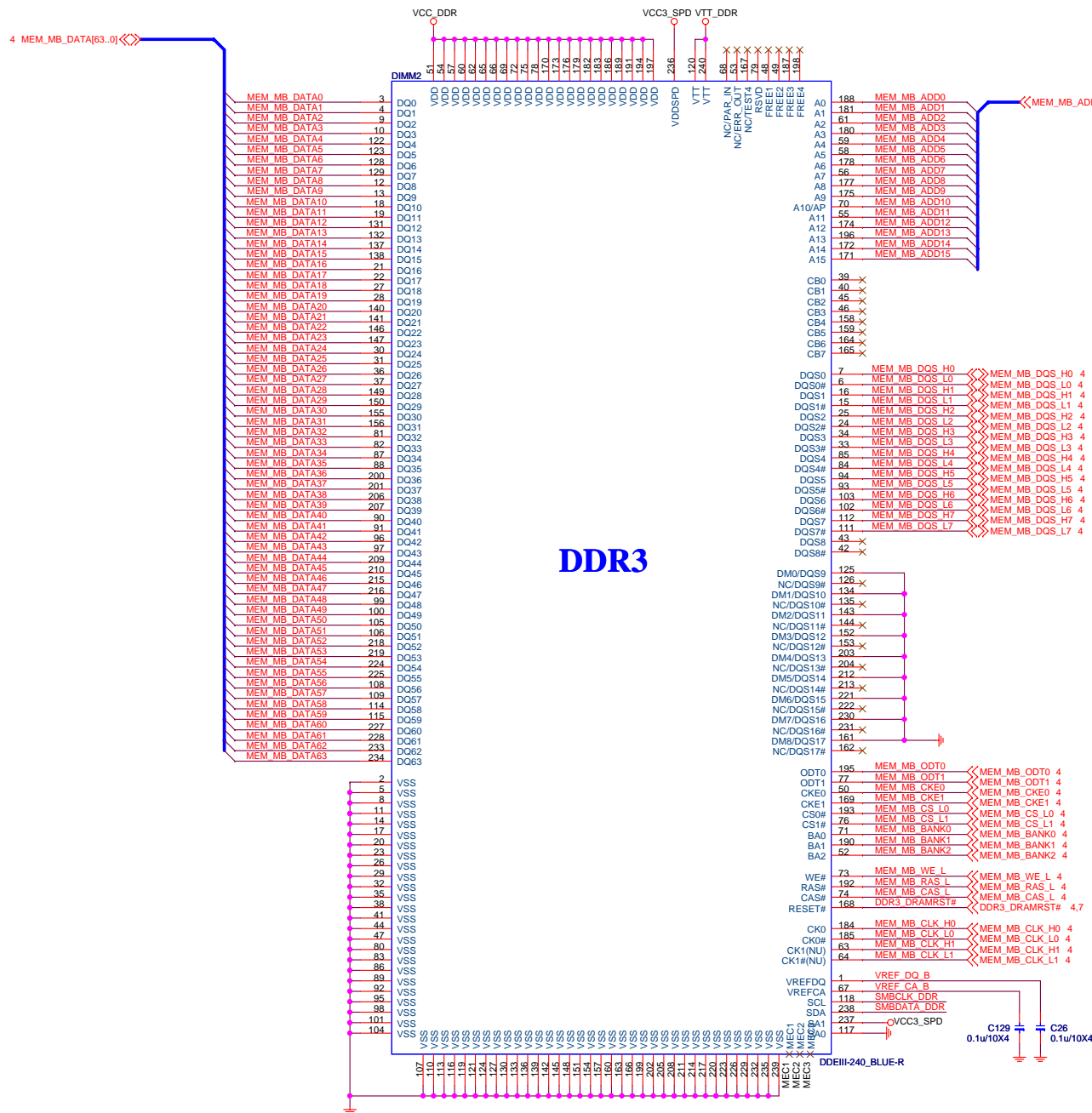


MICRO-STAR INT'L CO.,LTD		
MS-7817		
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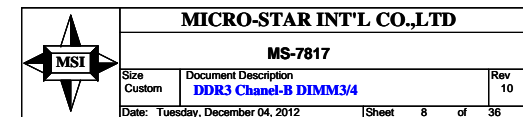
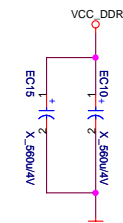
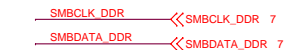
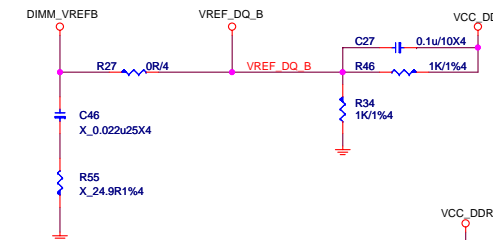
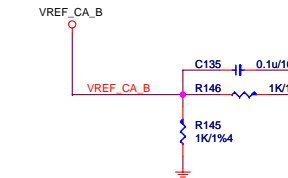
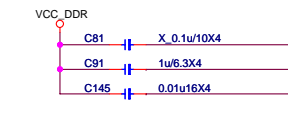
## DDRIII DIMM B0



Place close to DIMM2

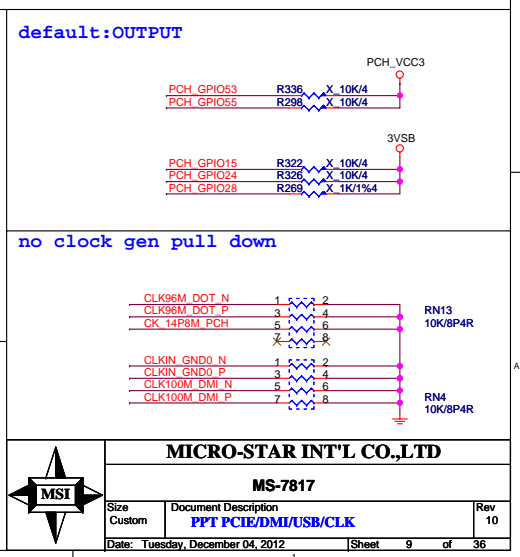
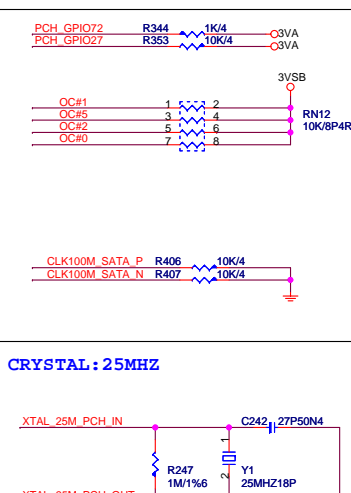
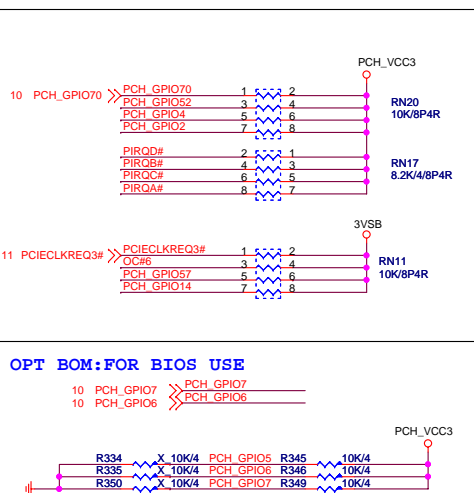
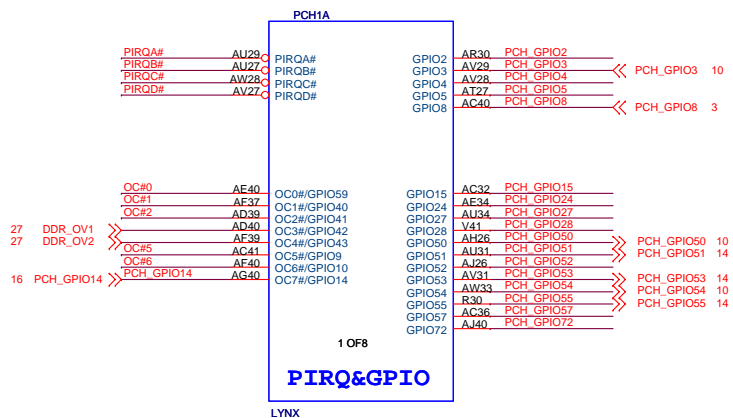


Place close to DIMM2





USB 2.0 ports 6,7,12 and 13 are disabled on 10 port SKUs.  
Only USB 3.0 ports 1 and 2 are enabled.  
pcie port7,8 NA



**MSI**

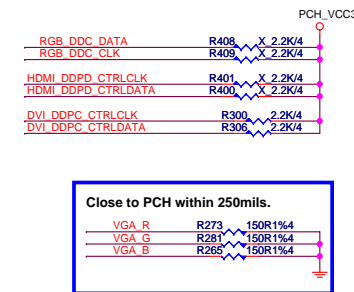
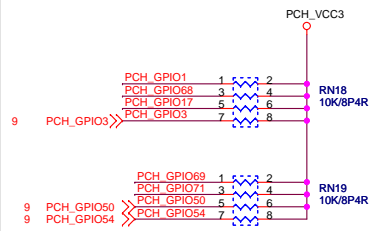
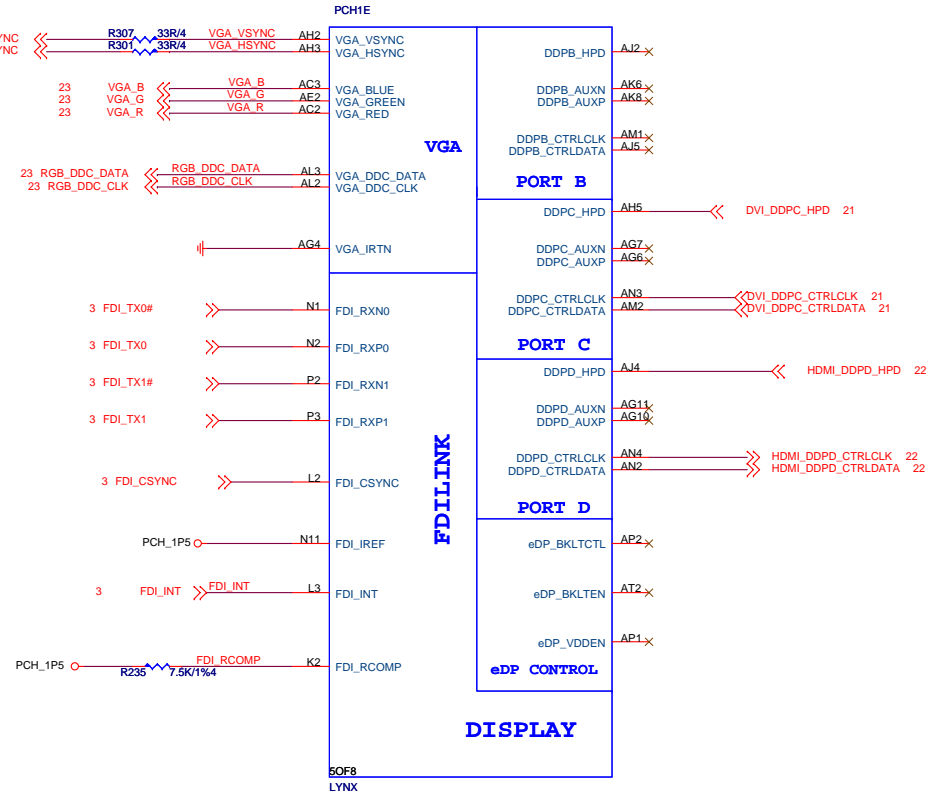
**MICRO-STAR INT'L CO.,LTD**

**MS-7817**

Size: Custom Document Description: PPT PCIe/DMI/USB/CLK Rev: 10

Date: Tuesday, December 04, 2012 Sheet: 9 of 36

SATA 6 Gb/s support on ports 0 and 1 only.

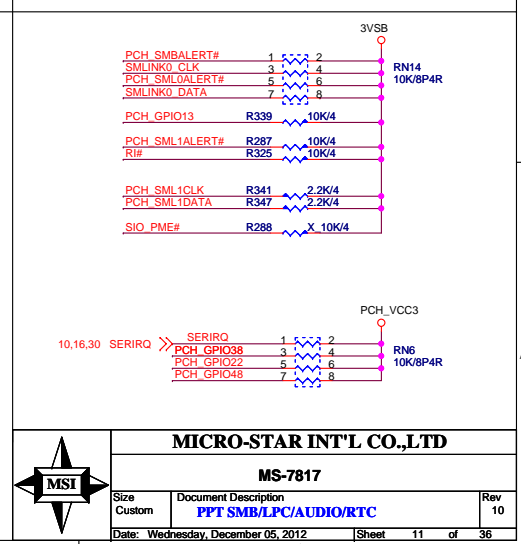
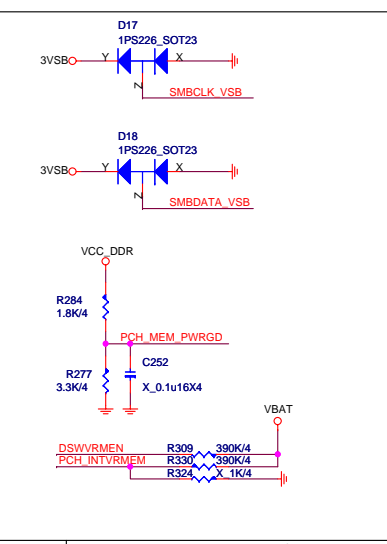
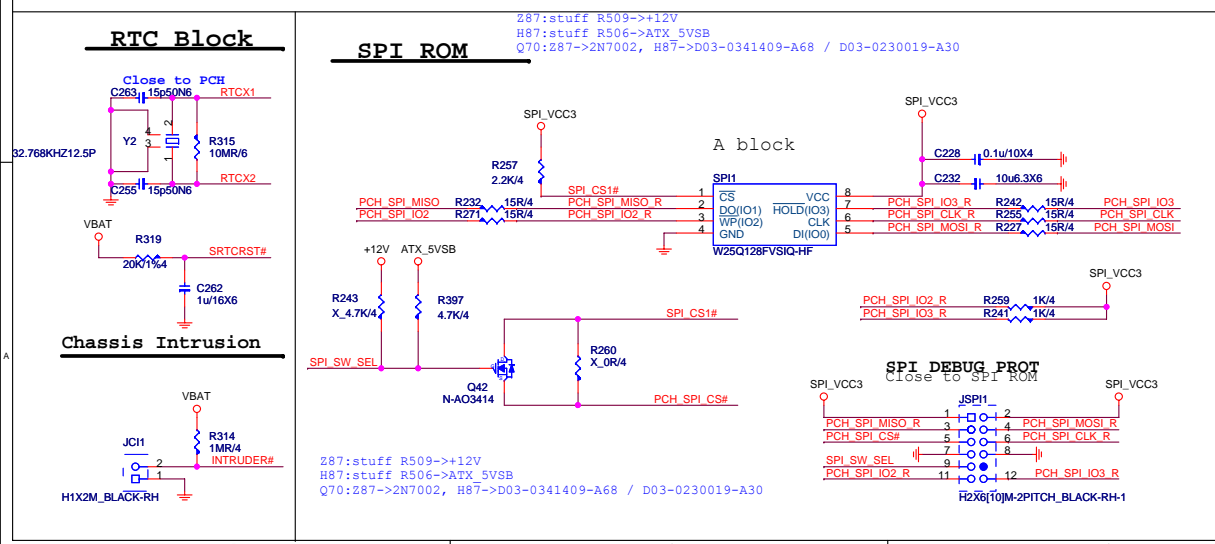
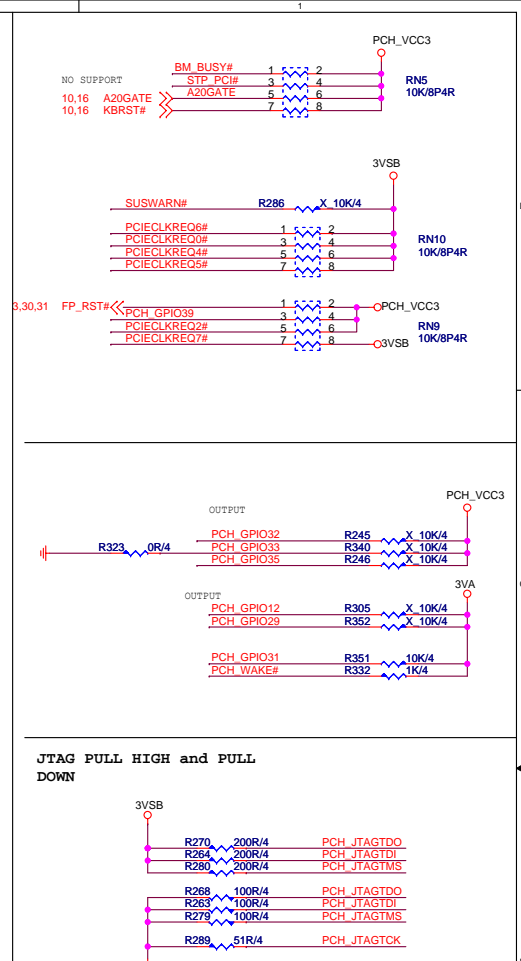
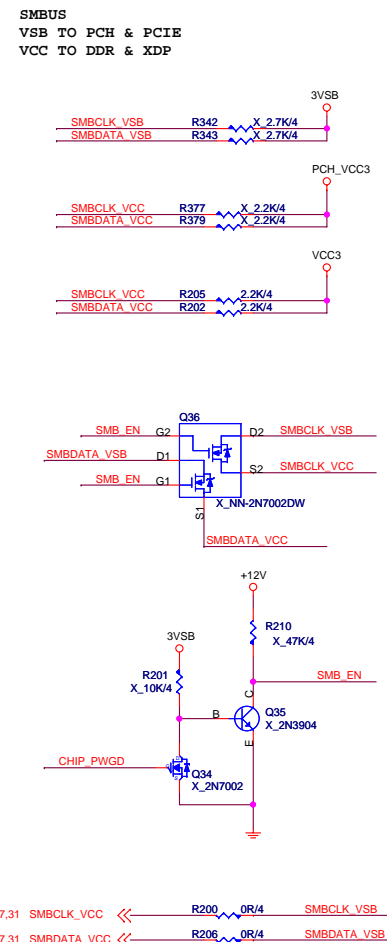


**MICRO-STAR INT'L CO.,LTD**

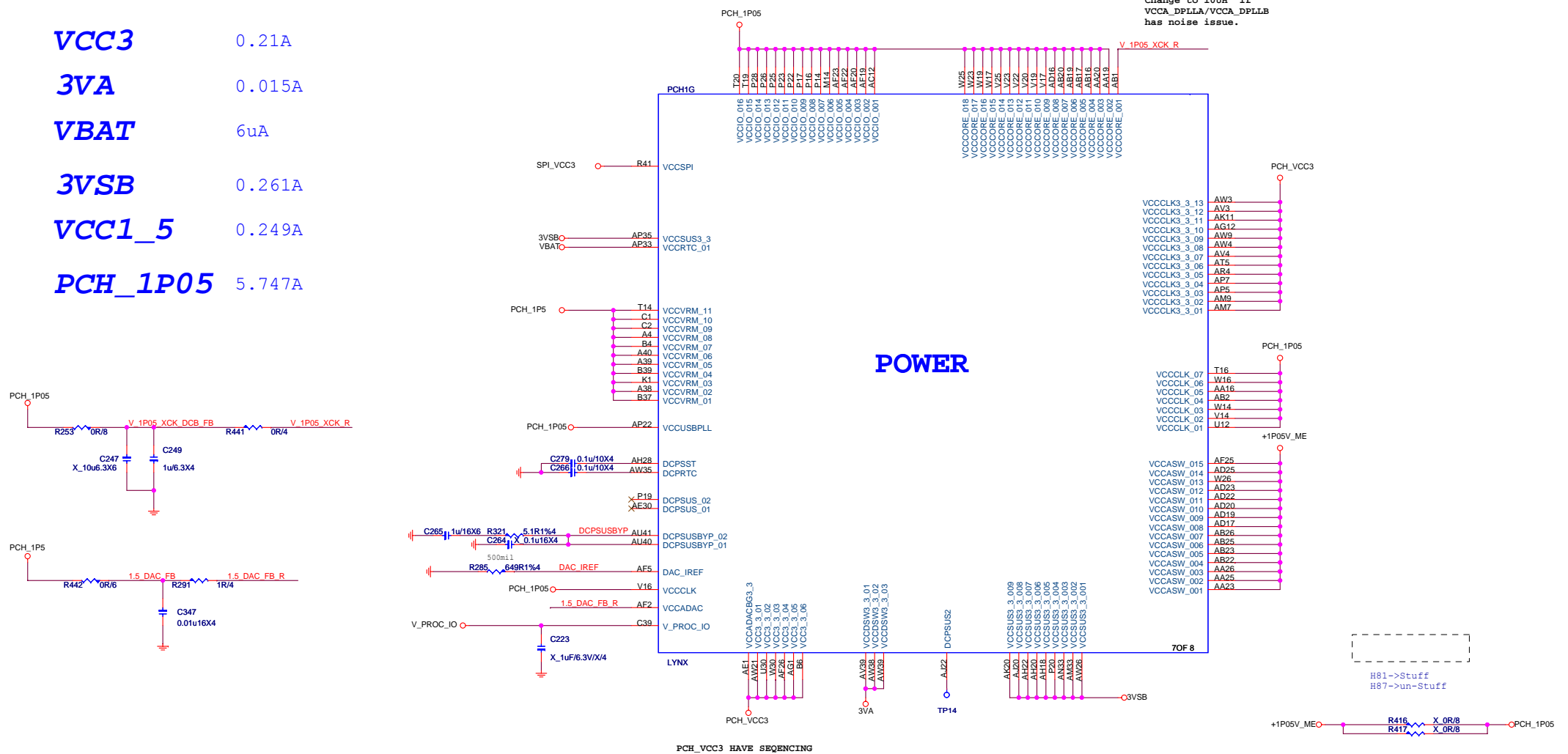
MS-7817

Size	Document Description
Custom	<b>PPT SATA/HOST/FAN/GPIO/VGA</b>

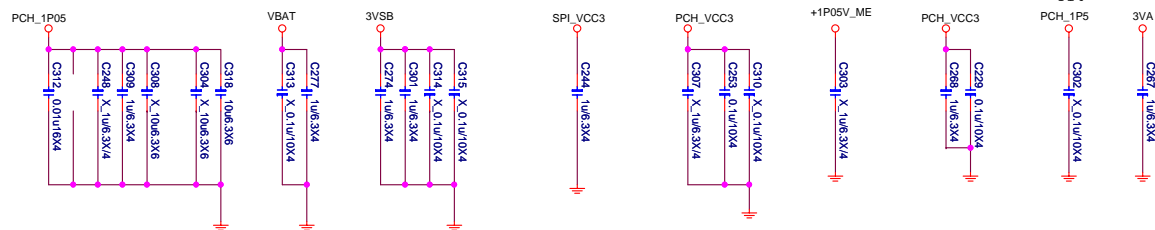
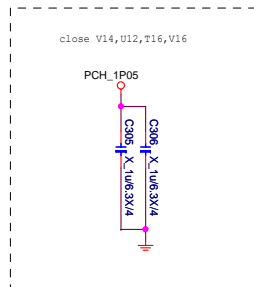
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<b><i>VCC3</i></b>	0.21A
<b><i>3VA</i></b>	0.015A
<b><i>VBAT</i></b>	6uA
<b><i>3VSB</i></b>	0.261A
<b><i>VCC1_5</i></b>	0.249A
<b><i>PCH_1P05</i></b>	5.747A



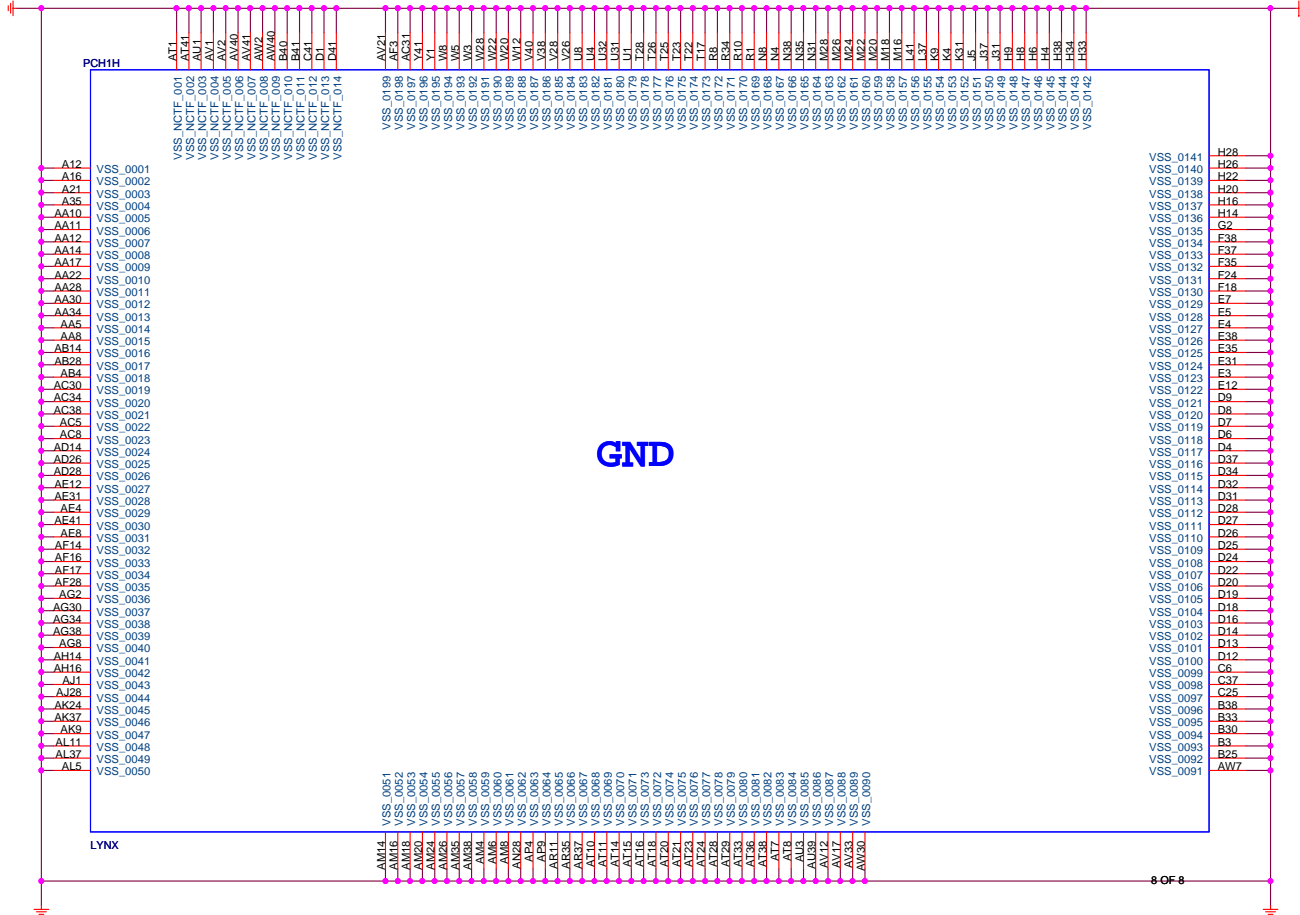
PCH decoupling cap



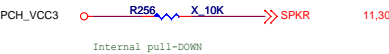
**MICRO-STAR INT'L CO.,LTD**

MS-7817

Size Custom	Document Description <b>LYNX -POWER PIN</b>	Rev 10
Date: Tuesday, December 04, 2012	Sheet 12 of 36	

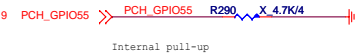


PCH Straps



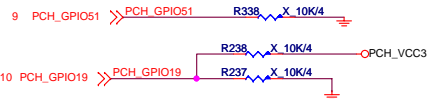
SPKR

Default Mode:  
Internal weak Pull-down.  
No Reboot Mode with TCO Disabled:  
Connect to Vcc3\_3 with 8.2k-10k Ohm weak pullup resistor.



GPIO55

Default Mode:  
Internal pull-up.  
Top Block Swap Mode:  
Connect to ground with 4.7k Ohm weak pulldown resistor.



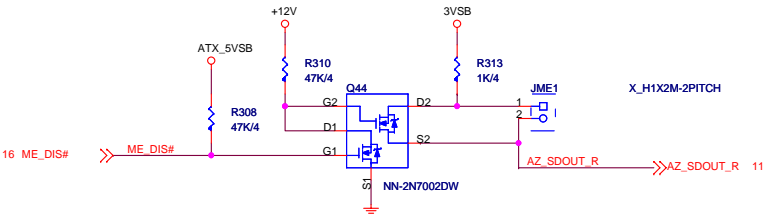
SATA1GF/GPIO19, GPIO51

Default (SPI):  
Left both SATA1GF/GPIO19 and GPIO51 floating.  
No pull up required.  
Boot from PCI:  
Connect SATA1GF/GPIO19 to ground with 1k Ohm pull-down resistor.  
Leave GPIO51 Floating.  
Boot from LPC:  
Connect both SATA1GF/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



GPIO53

Do not pull low.  
Connect to ground with 1k Ohm pull-down resistor.



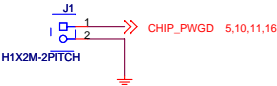
HDA\_SDO

Default:  
Do not pull high.  
Disable ME in Manufacturing Mode:  
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

GPIO37

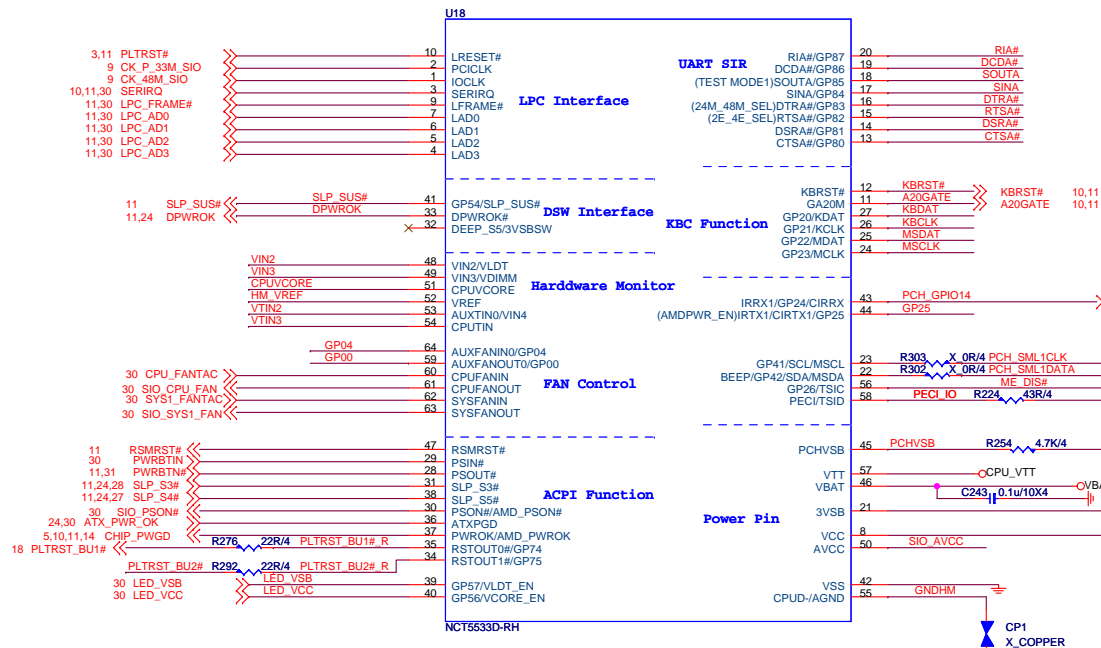
Enable TLS:  
Pull up with 1k Ohm to VccSus3.3.  
Default (Disable TLS):  
Leave NC. Internal pull down.

For test cpu voltage

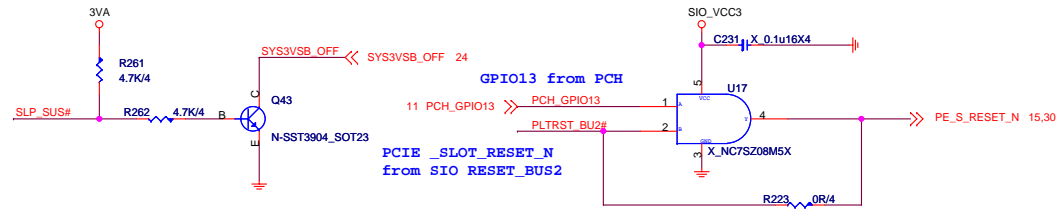




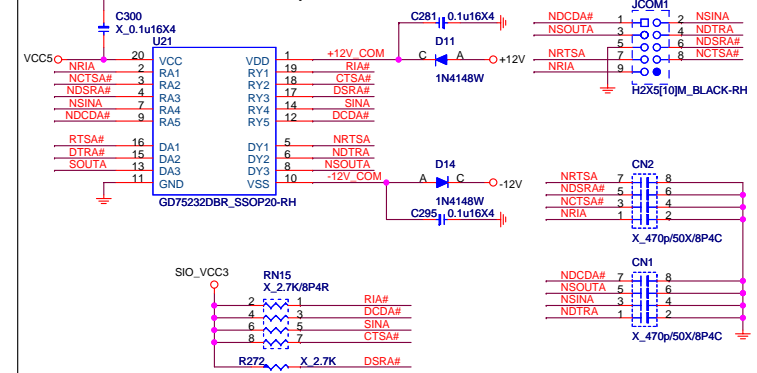




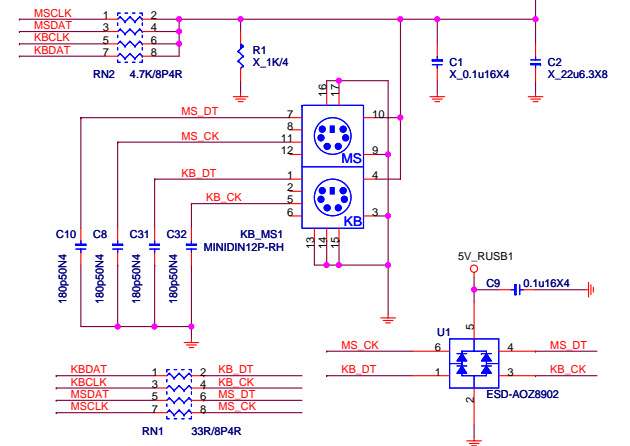
### 5533D DSW SUPPORT



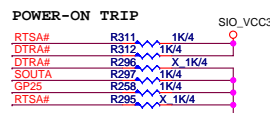
### SERIAL PORT 1



### PS2 Connector



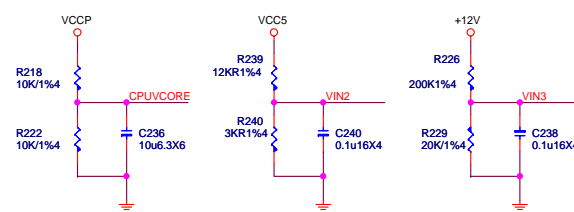
### LPC I/O STRAPPING RESISTOR



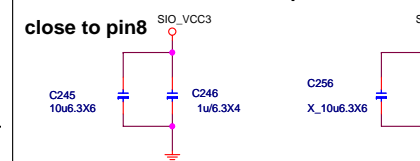
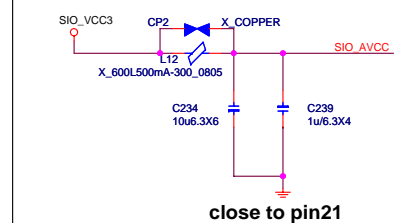
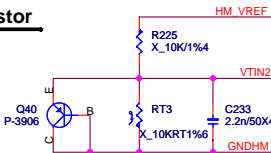
### NCT5533D POWER ON STRAPPING PIN

PIN	Function	NET Name	HI	LO
44	AMD_PWR_EN		ENABLE AMD PWR SEQ	DISABLE AMD PWR SEQ
18	TEST_MODE1	SOUTA	TEST MODE 1 ENABLE	TEST MODE 1 DISABLE
16	24M_48M_SEL	DTRA#	48MHz	24MHz
15	2E_4E_SEL	RTSA#	4E	2E

### Voltage Sensing

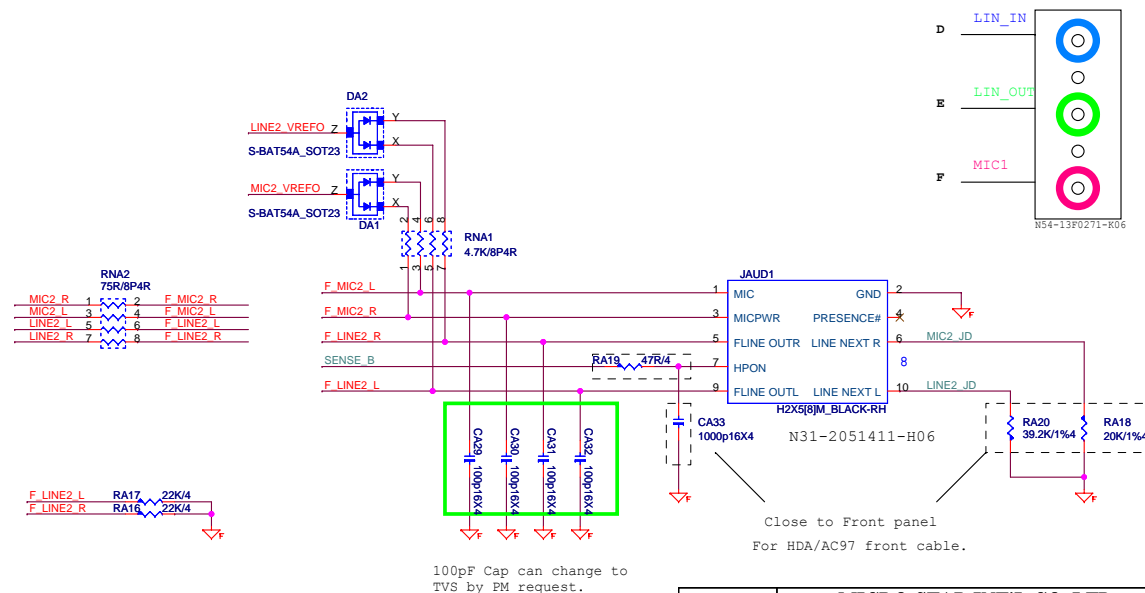
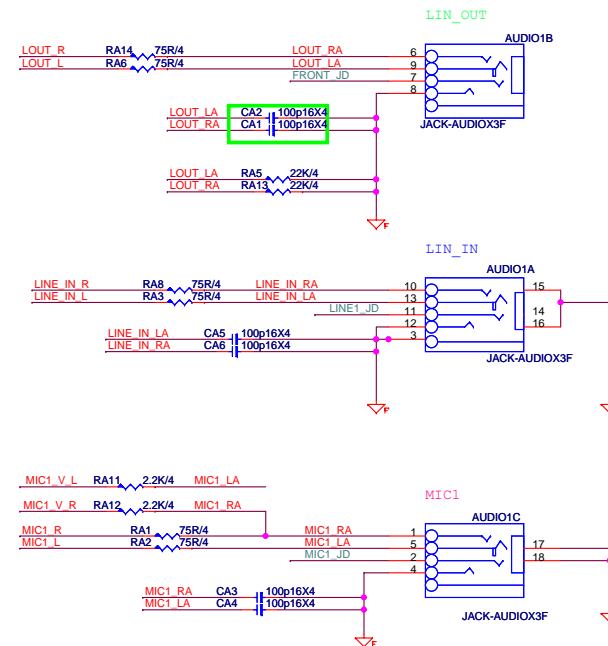
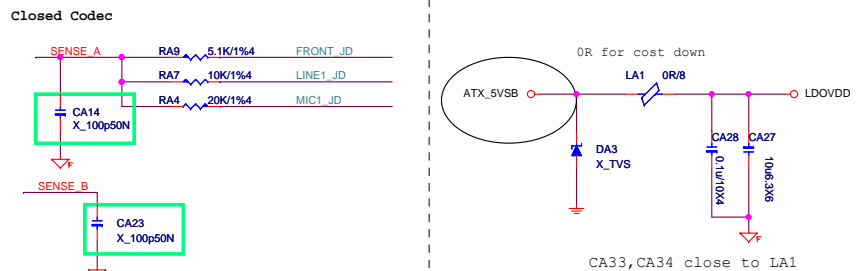
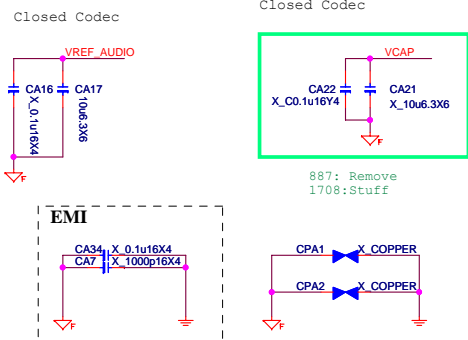
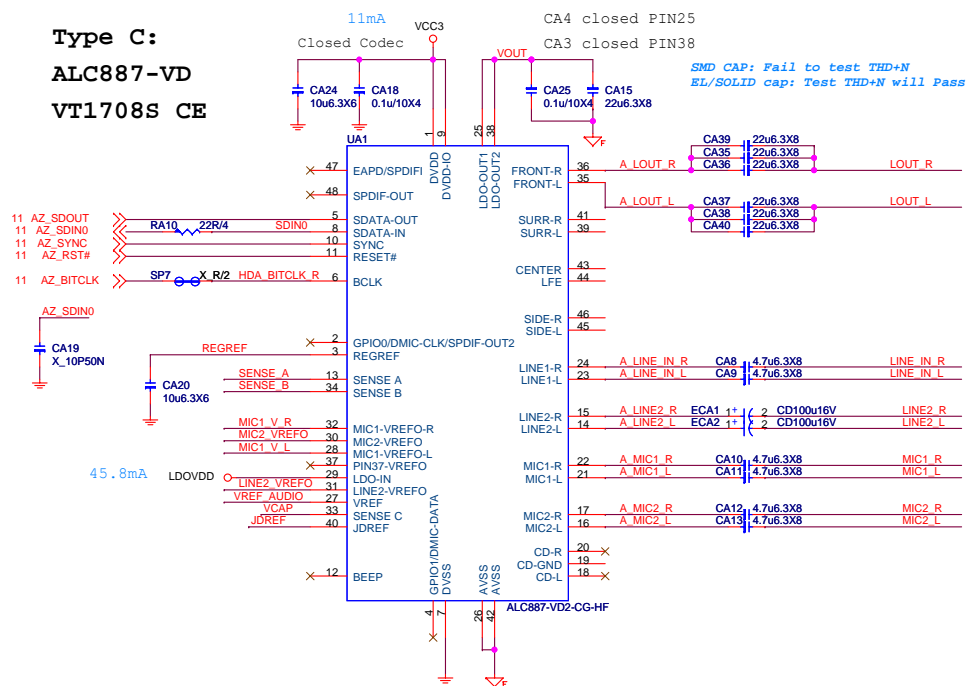


### Thermal Resistor



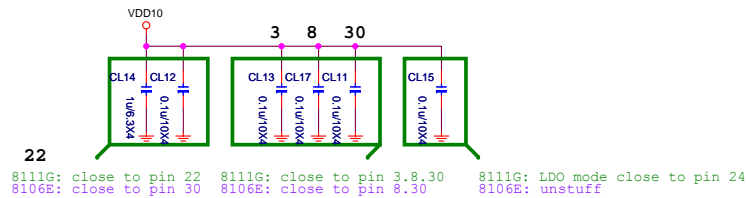
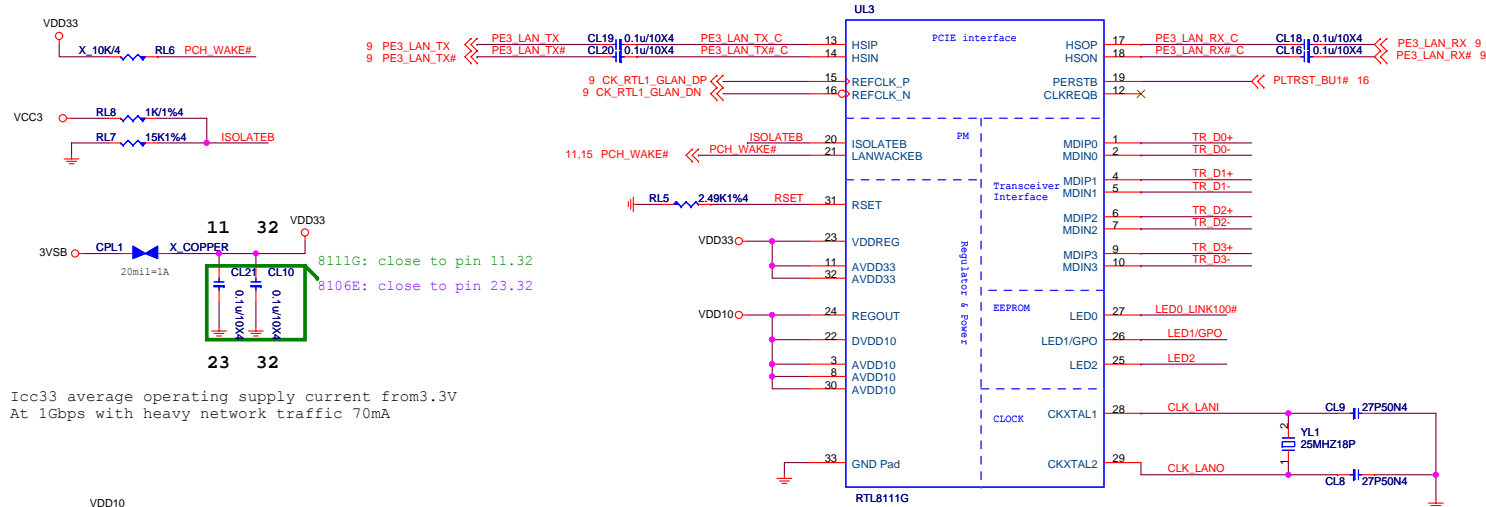
**MICRO-STAR INT'L CO.,LTD**  
**MS-7817**  
Size Custom | Document Description **SIO-NUVOTON NCT5533D** | Rev 10  
Date: Tuesday, December 04, 2012 | Sheet 16 of 36

Type C:  
ALC887-VD  
VT1708S CE

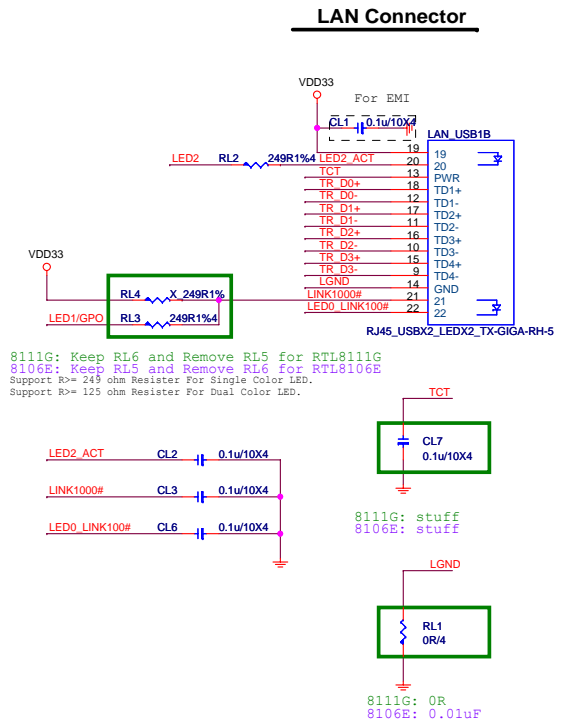


<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7817</b>			
Size Custom	Document Description <b>Audio Codec ALC892/887</b>		Rev 10
Date: Tuesday, December 04, 2012		Sheet	17 of 36

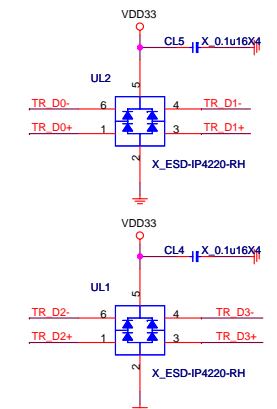
```
RTL8111G Giga LAN
RTL8106E 10/100M LAN
```



Icc10 average operating supply current from 1.0V  
At 1Gbps with heavy network traffic 300mA



## Reserve ESD Protect

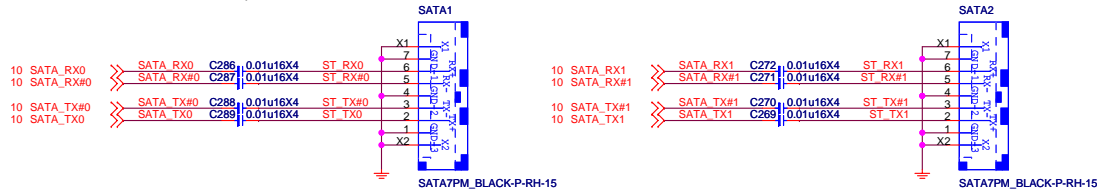


**MICRO-STAR INT'L CO.,LTD**

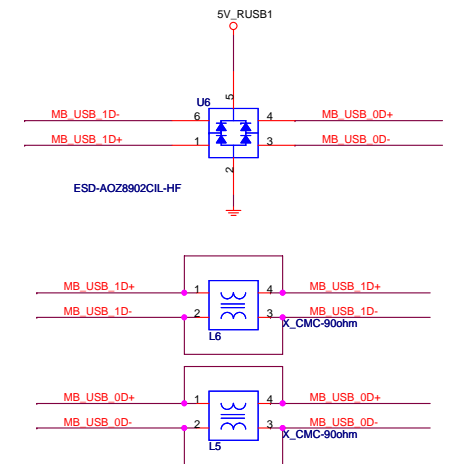
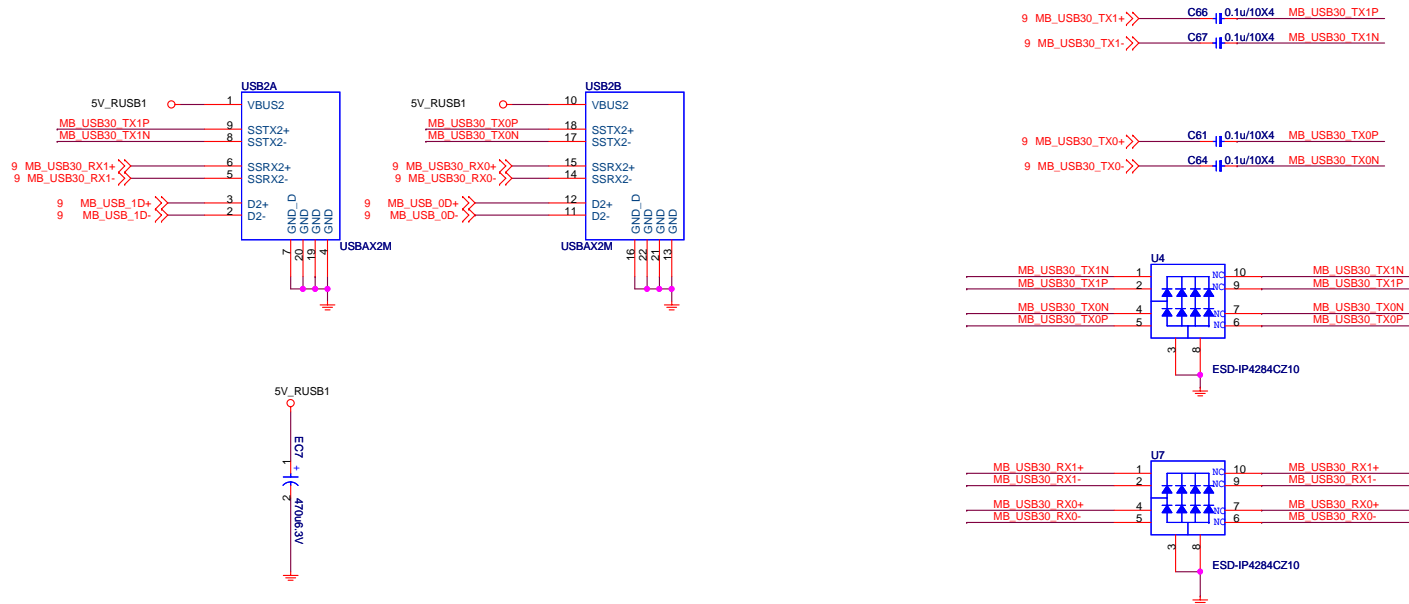
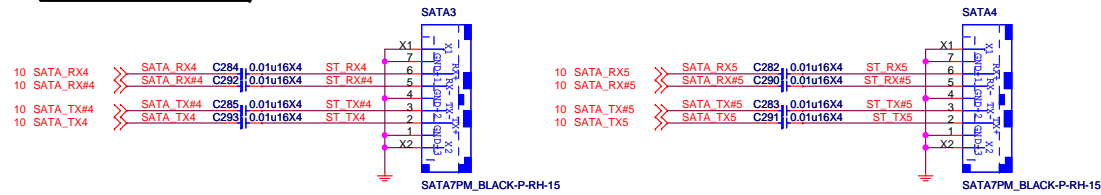
MS-7817

Size Custom	Document Description <b>LAN RTL8111G/8106E</b>	Rev 10
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**SATA 6G PORT 0,1**



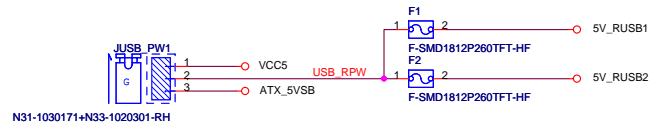
**SATA 3G PORT 4,5**



# Type C: jumper +Fuse

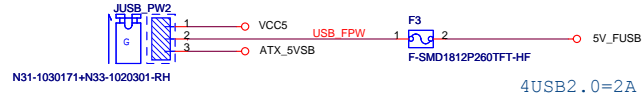
PCH/FCH side: OC# pull high to +3VSB

Near Rear ==>



$$4USB2.0+2USB3.0+PS2=5A$$

Near Front ==>

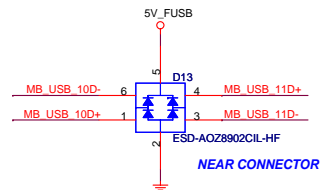
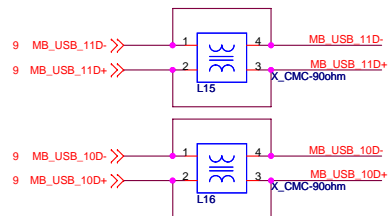


## Default VCC5 (PIN1-2)

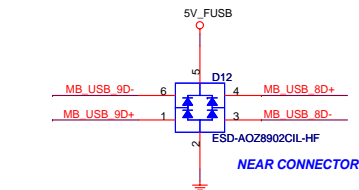
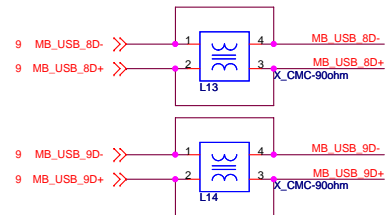
JUSB_FW	BIOS Menu	Wake up support
1-2	EUP Enable	Not support
	EUP Disable	Not support
2-3	EUP Enable	Not support
	EUP Disable	support

D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)  
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)  
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)

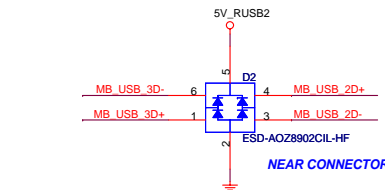
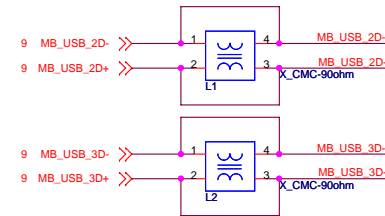
## FRONT USB PORT 8,9



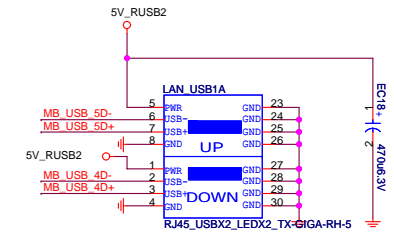
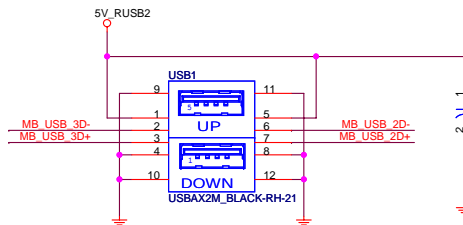
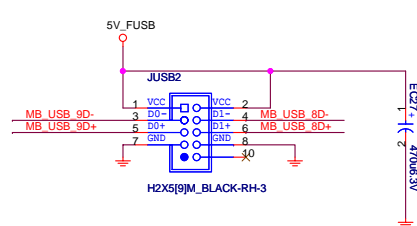
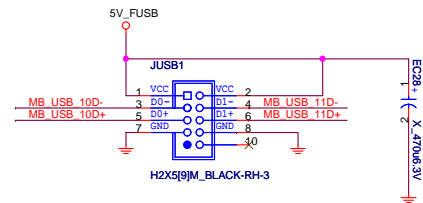
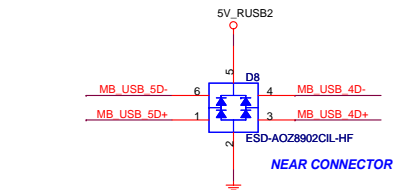
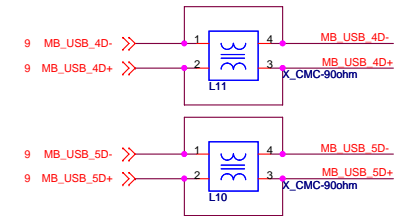
## FRONT USB PORT 10,11



## FRONT USB PORT 10,11

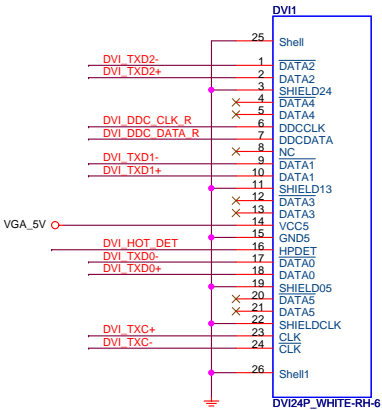
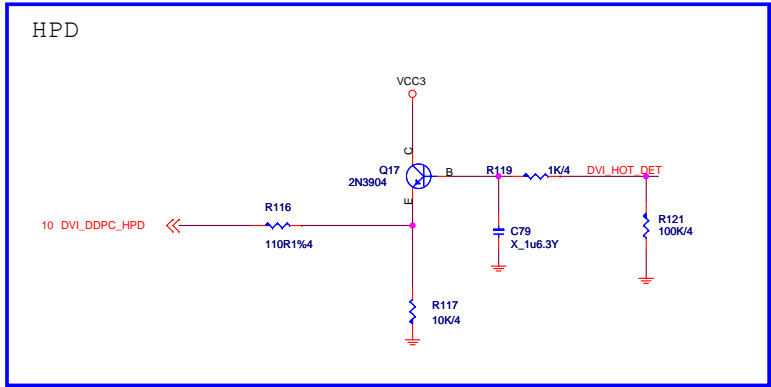
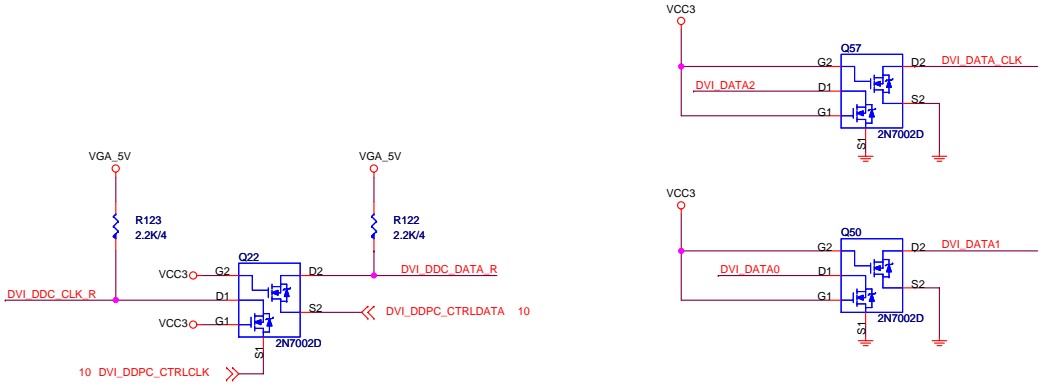
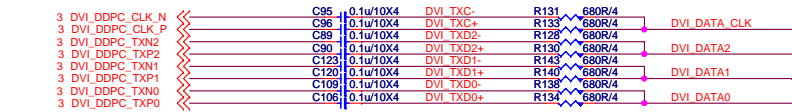


## FRONT USB PORT 10,11

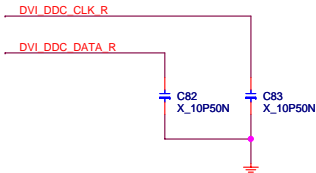
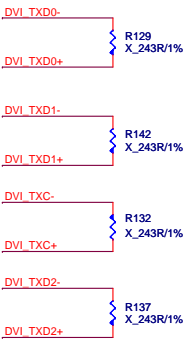


DVI level shifter

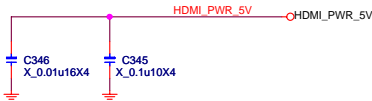
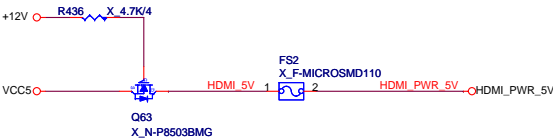
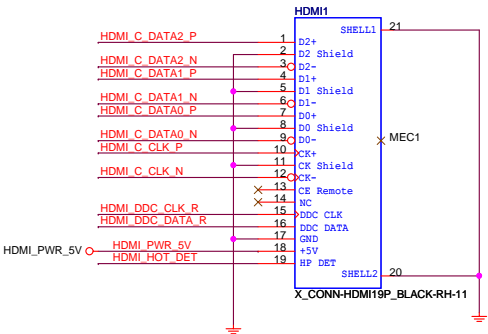
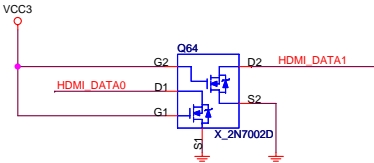
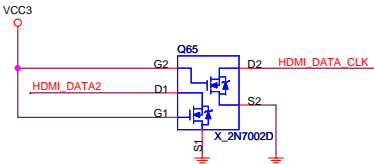
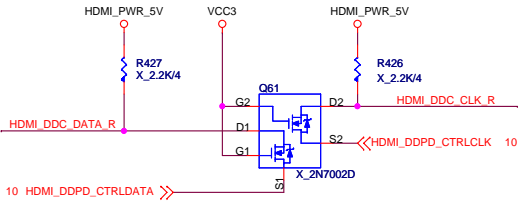
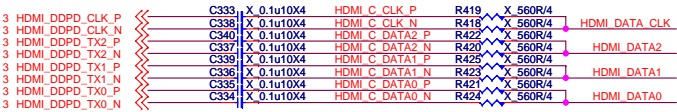
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



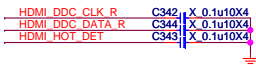
For EMI



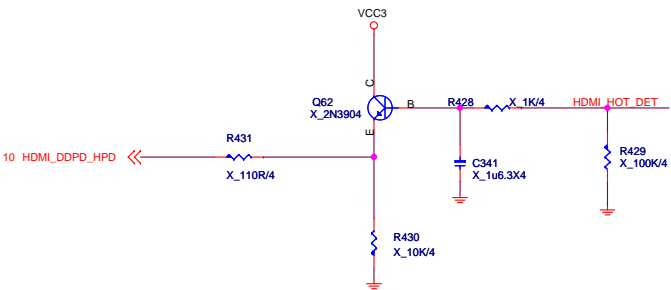
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



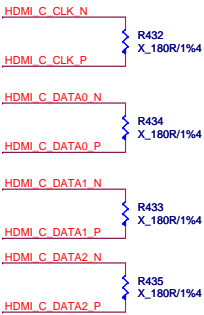
EMI



HPD



For EMI



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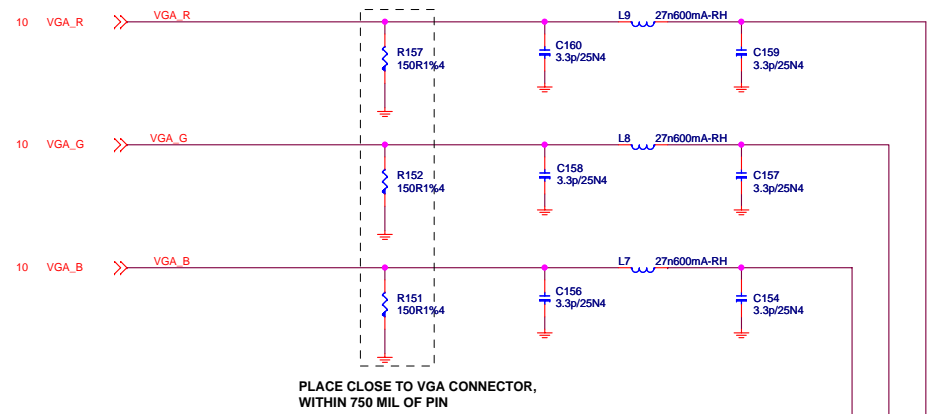
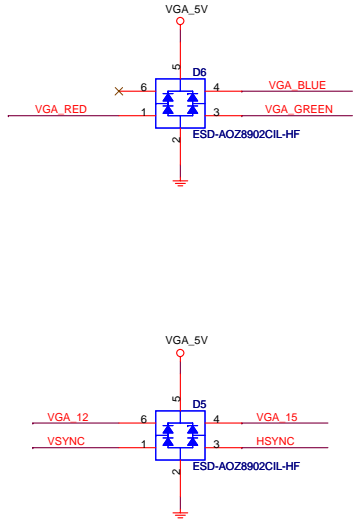
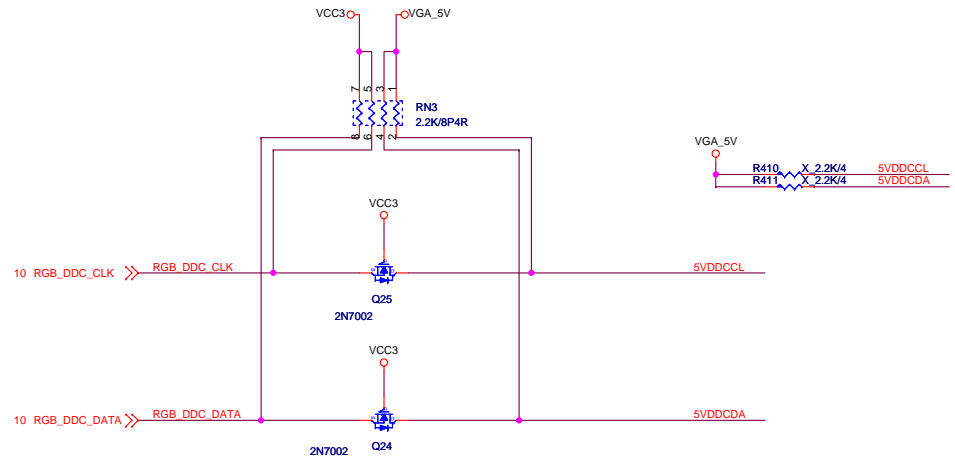
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Custom	HDMI Connector	10
Date: Wednesday, December 05, 2012	Sheet 22 of 36	

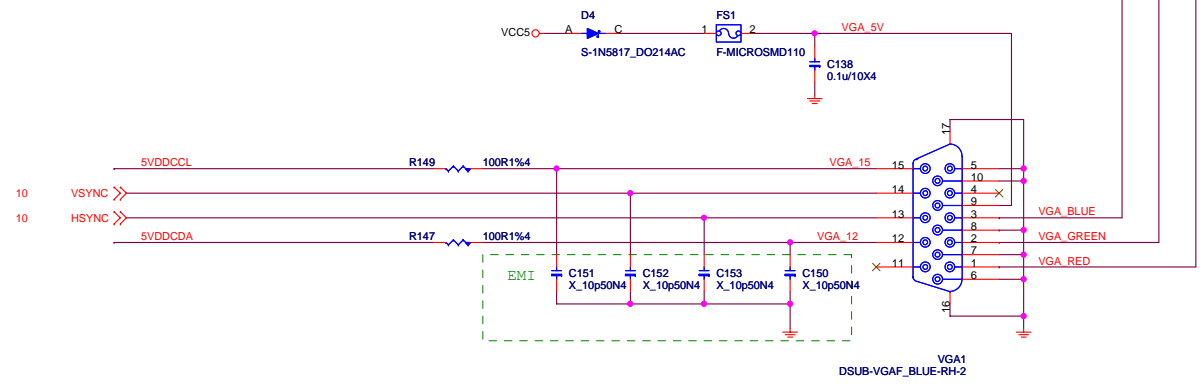


D-Sub

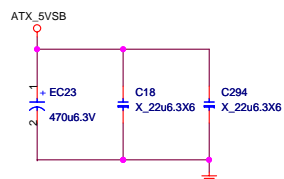
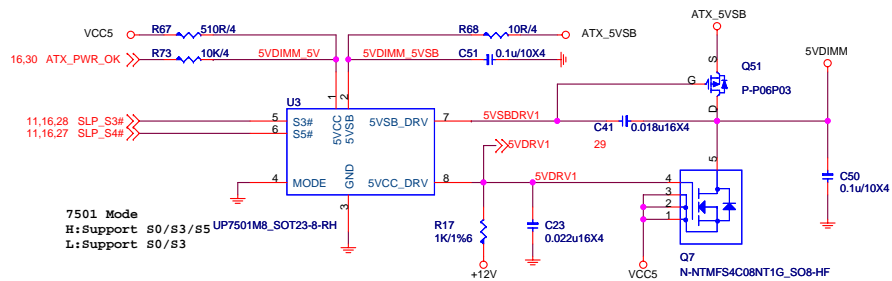
Level shift



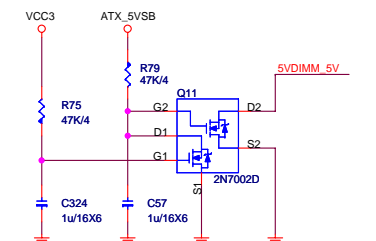
PLACE CLOSE TO VGA CONNECTOR,  
WITHIN 750 MIL OF PIN



## 5VDIMM FOR DDR



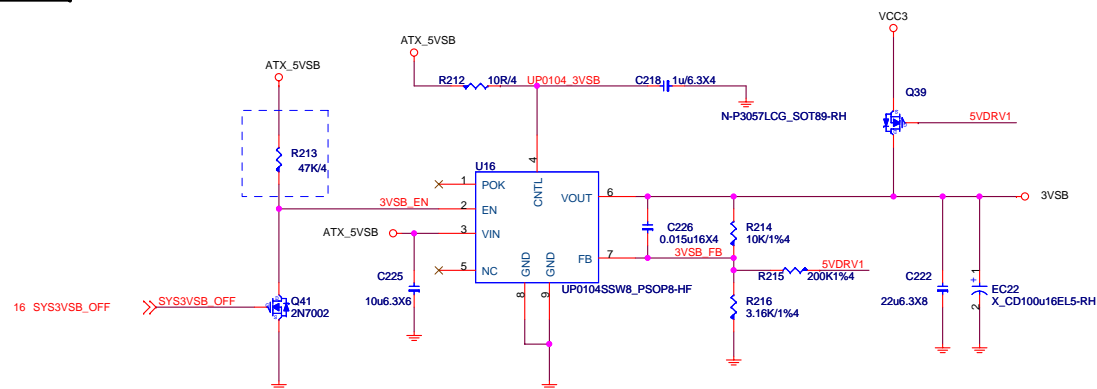
```
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.
```



## Patch coolermaster 700w power sequence

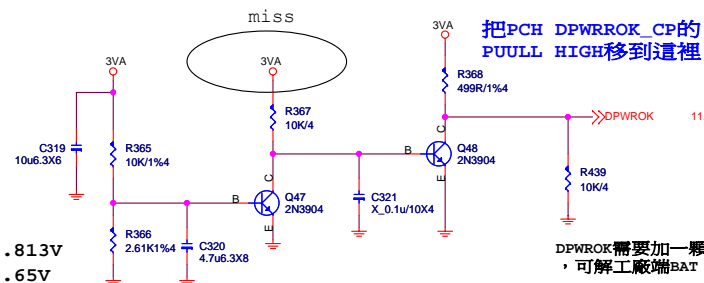
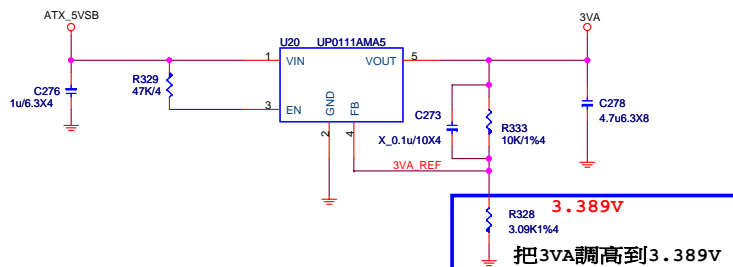
### 3VSB

3VSB supply to PCH and other device.  
Turn off when Deep S3/S5 by 5VSB off.



3VA

20mA



DPWROK需要加一顆pull down 10k電阻  
，可解工廠端BAT 電流過大問題

FOR DPWROK跟3VA的POWER  
DOWN的時序(S5-->G3)

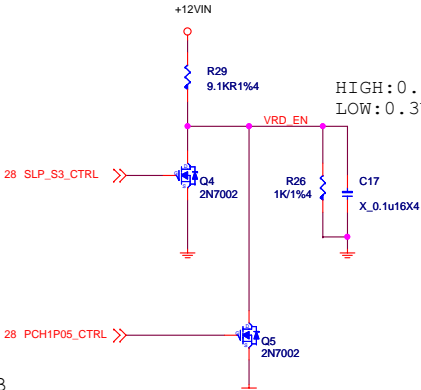


**MICRO-STAR INT'L CO.,LTD**

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Size Custom	Document Description <b>ACPI controller UPI</b>	Rev 10
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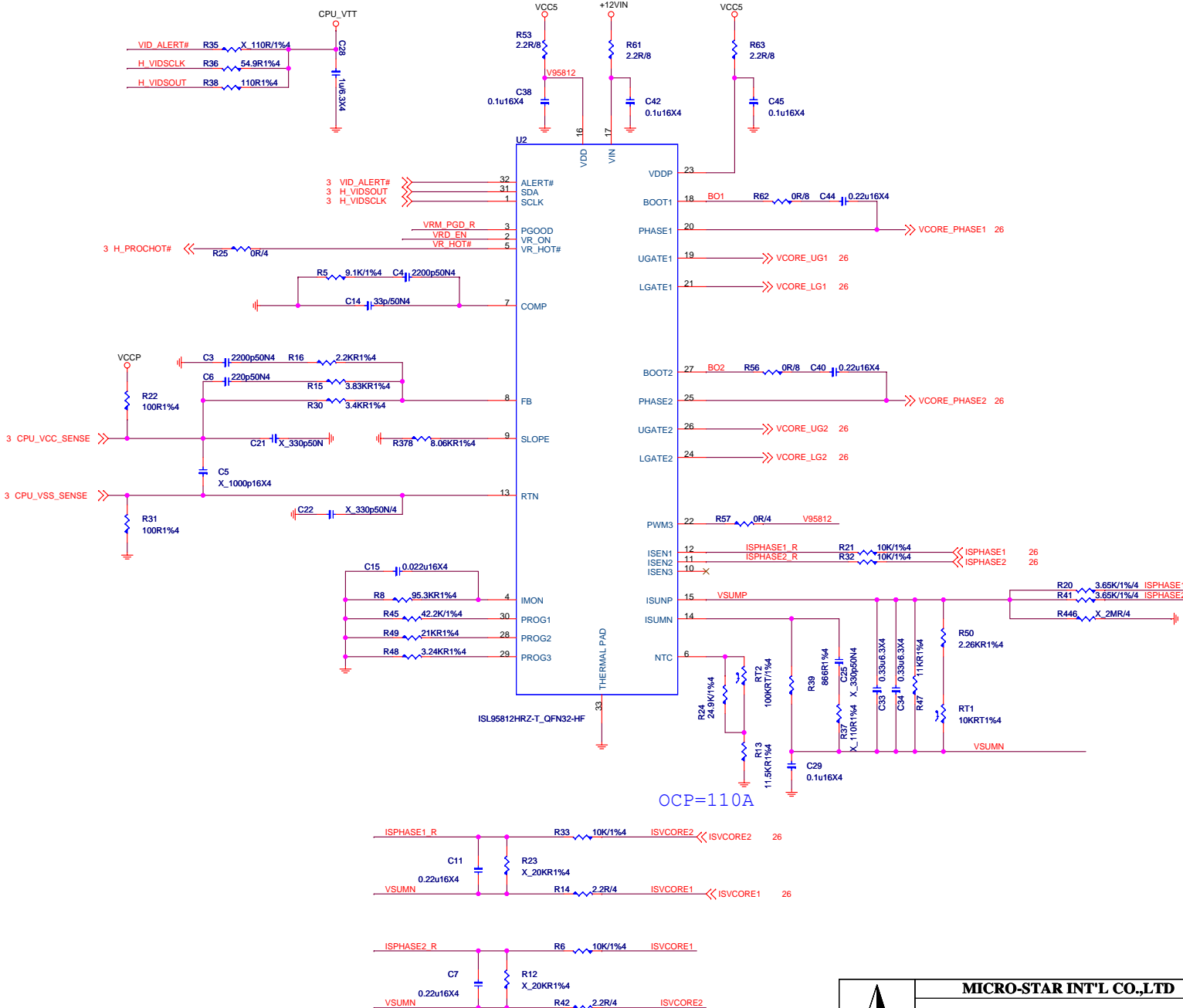
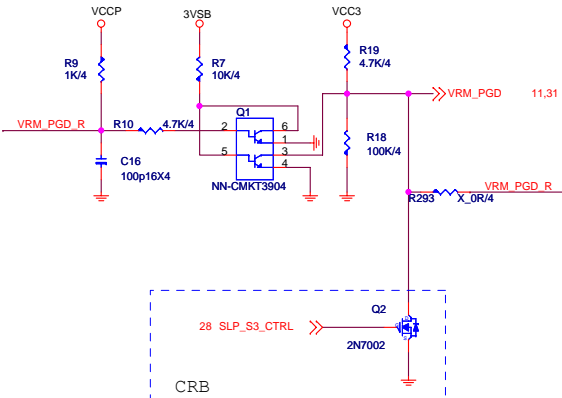
VCORE power on by s3 and 12v



CRE

HIGH:by PCH\_1P05V  
LOW:by S3

## VRMPWRGD LEVEL SHIFT



**MICRO-STAR INT'L CO.,LT**

**MS-78**

Size	Document Description
Custom	<b>VRD12.5 - ISL958</b>

Rev	10
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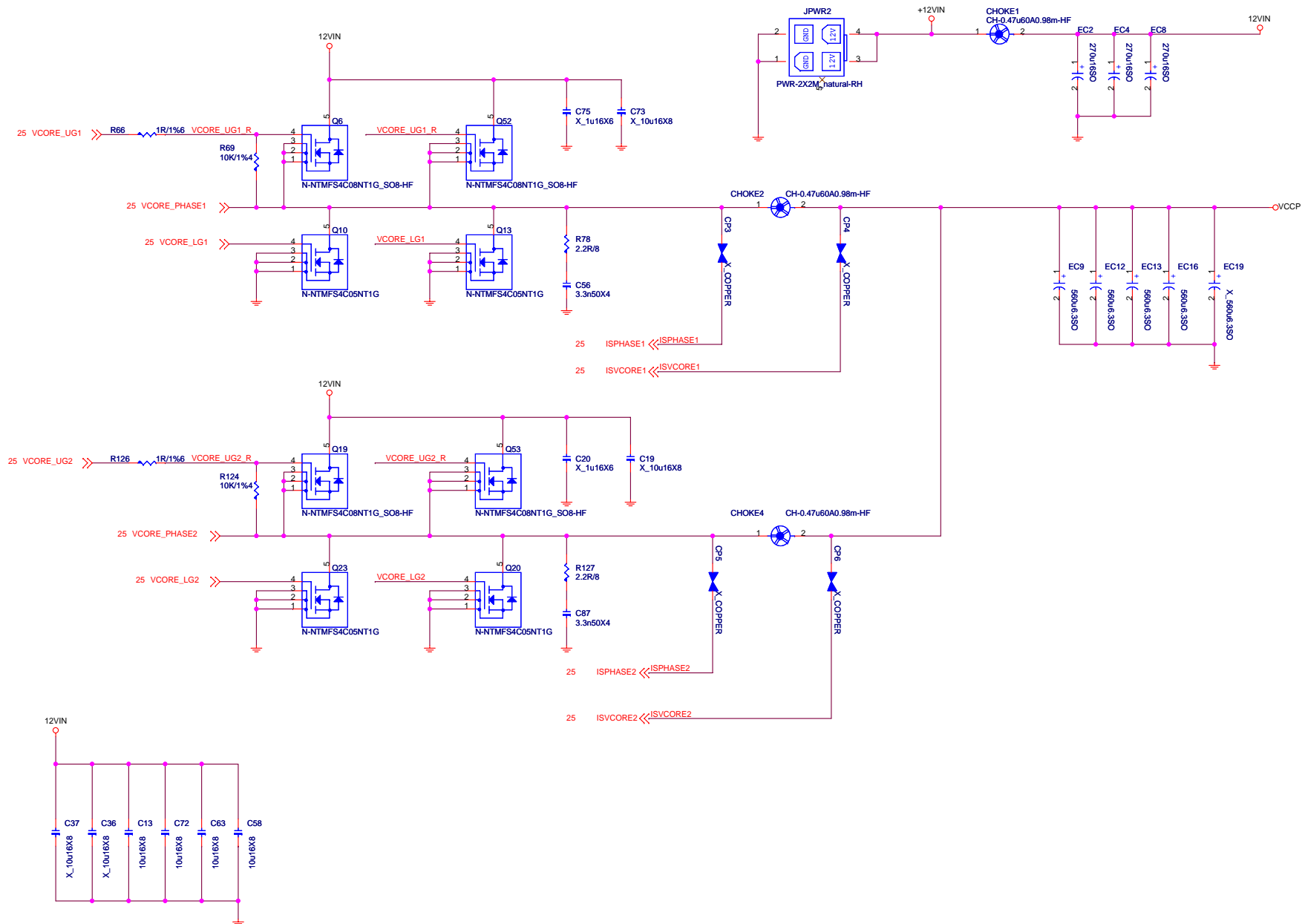
Date: Tuesday, December 04, 20

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# VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W  
LL:2.5m ohm



# DDR Power:1.5V

DDR3\_1.5V 4.2A+6A+0.5A+7.661=18.361A OCP:66.7A

4.2A FOR CPU

6A FOR 2DIMM

0.5A FOR DDR VTT

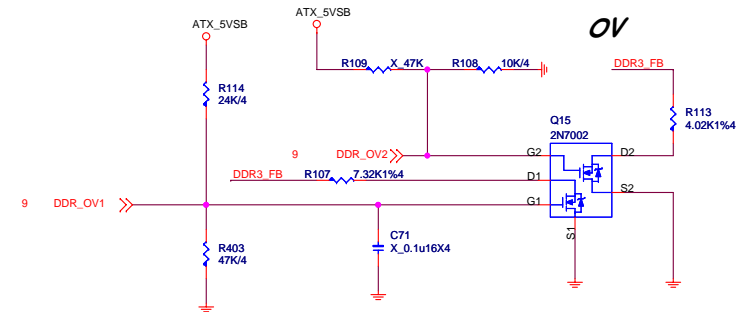
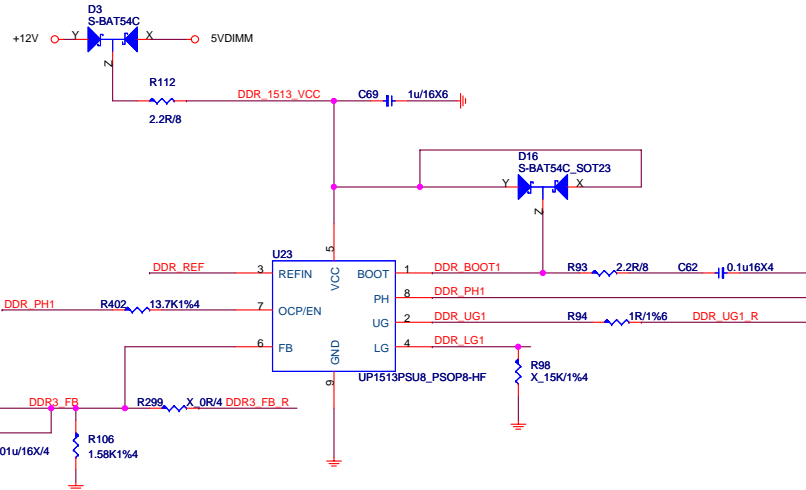
7.661A FOR PCH

$$OCP:16.447*1.5=24.6705A$$

$$OCPXRdson(Low\ side)=(40uA*Rocs(R122)-0.4V)$$

$$Rocs(R122)=13.75K$$

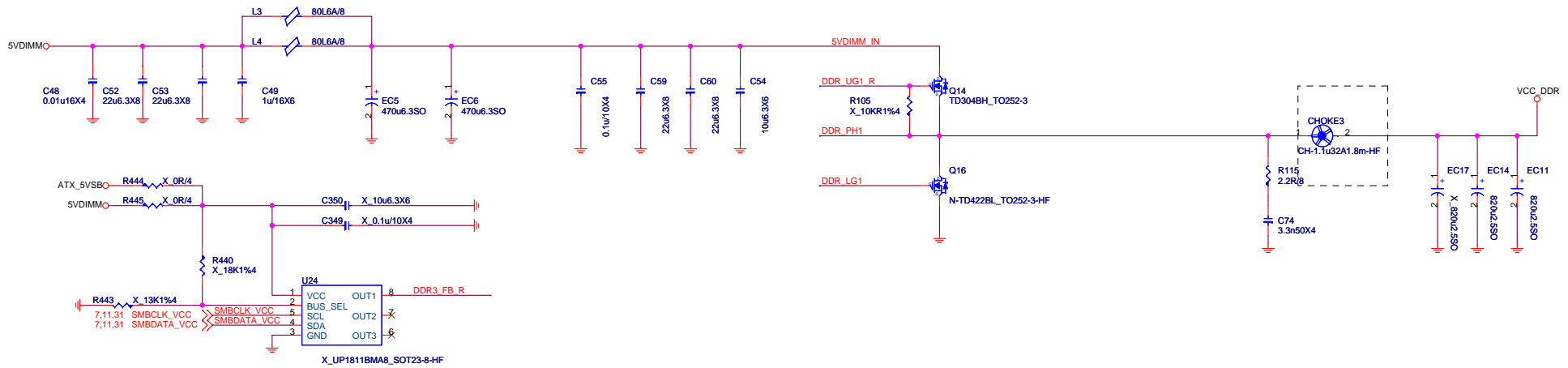
2012.03.22 Modify Pull hi (47K) to ATX\_5VSB



\*Default 1.5V

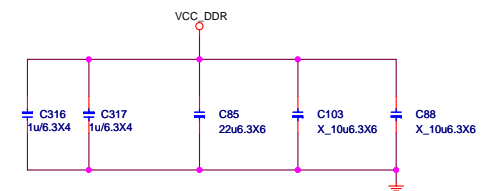
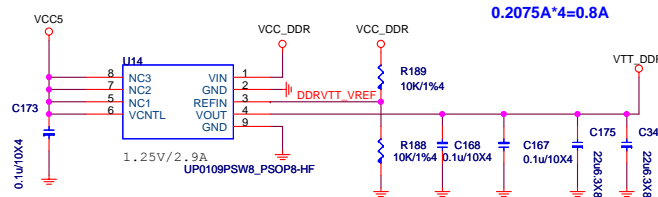
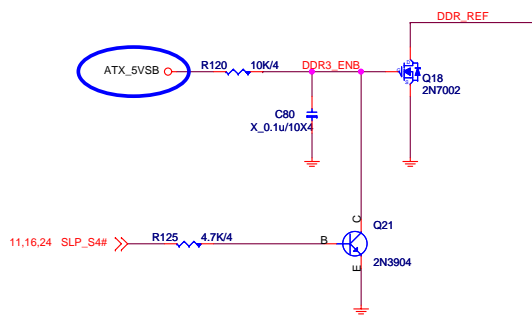
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR\_OV1 = GPIO01 (S/IO)  
DDR\_OV2 = GPIO02 (S/IO)



## DDR VTT Power

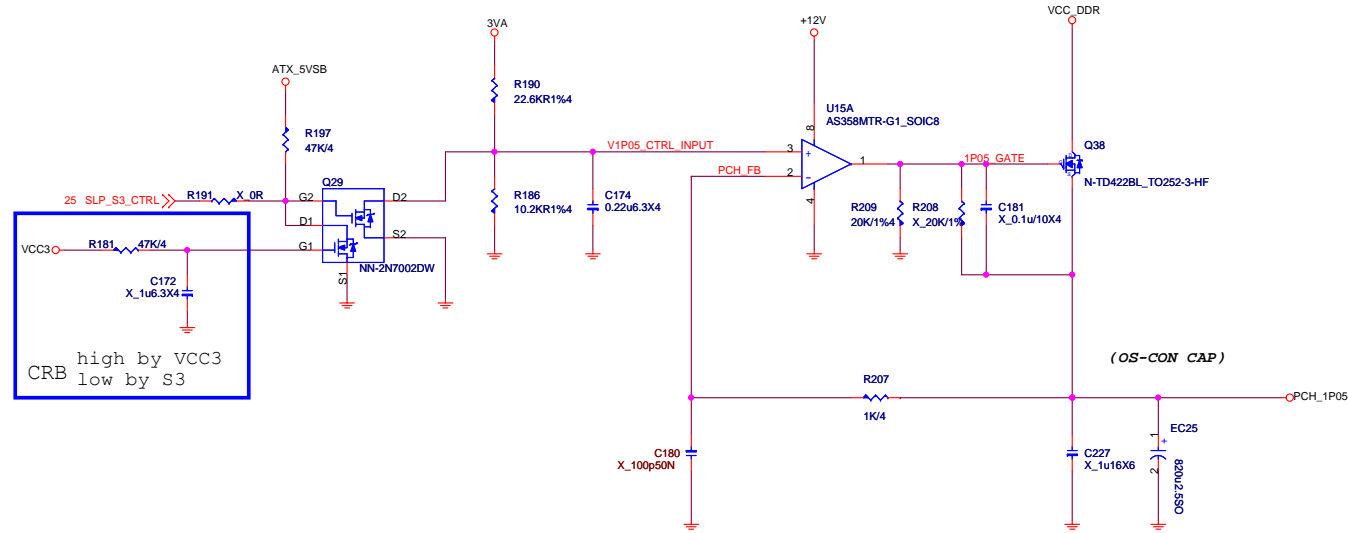
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



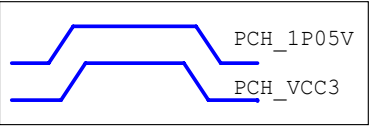
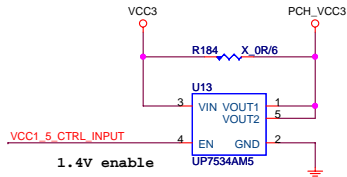
MICRO-STAR INT'L CO.,LTD			
MS-7817			
Size	Custom	Document Description	DDR Power - UP6103 1-Phase
Date:	Tuesday, December 04, 2012	Sheet	27 of 36

P.S. Only for meet Intel power down sequence.

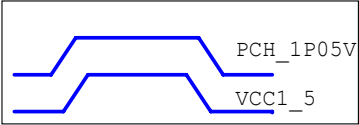
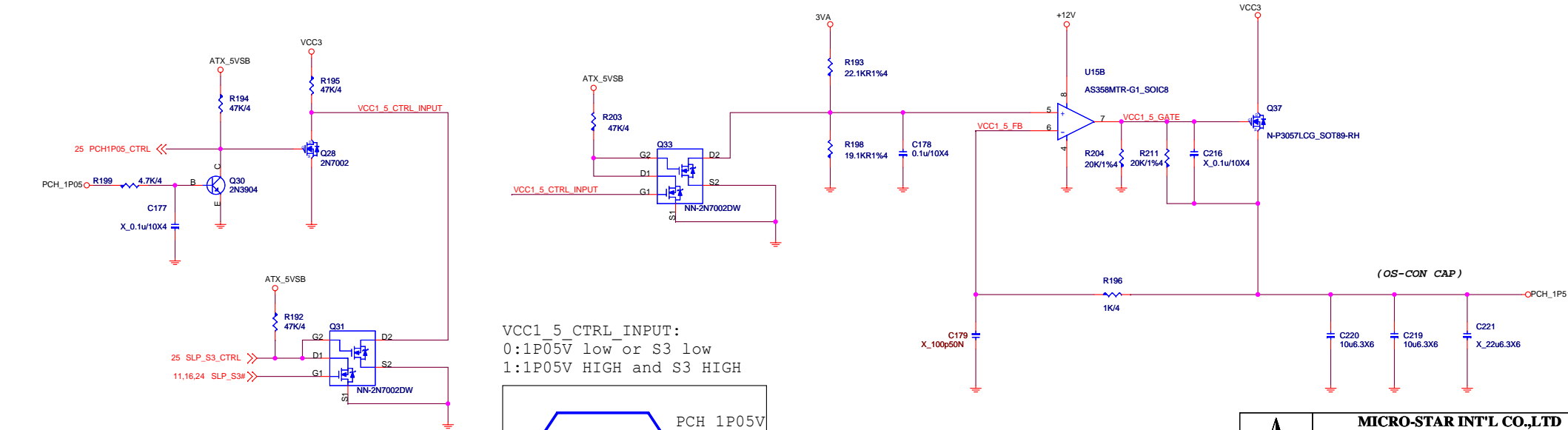
PCH Power:1.05V 5.747A



0.133A



PCH Power:1.5V 0.183A

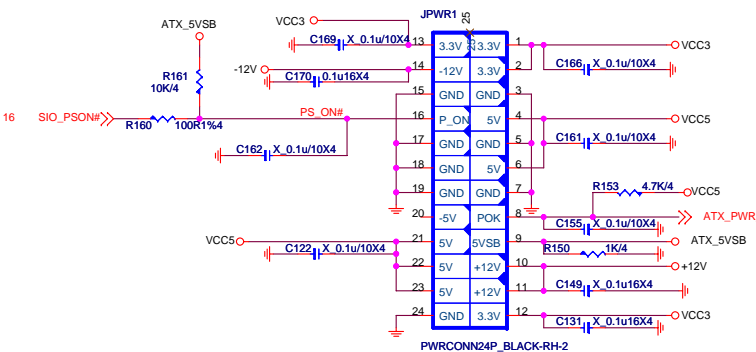


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MS-7817		
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Custom	PCH Power - OP+MOS	10
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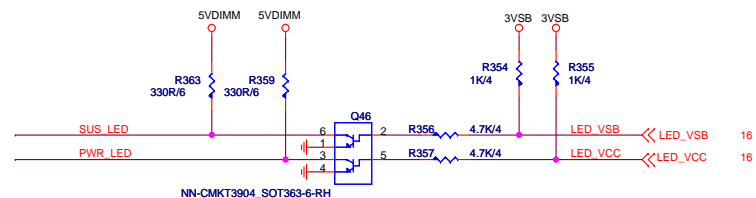




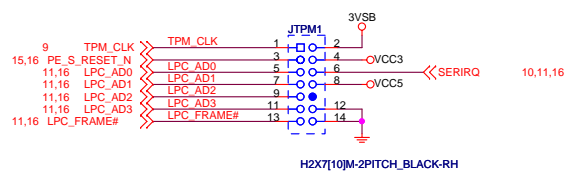
## ATX POWER CONNECTOR



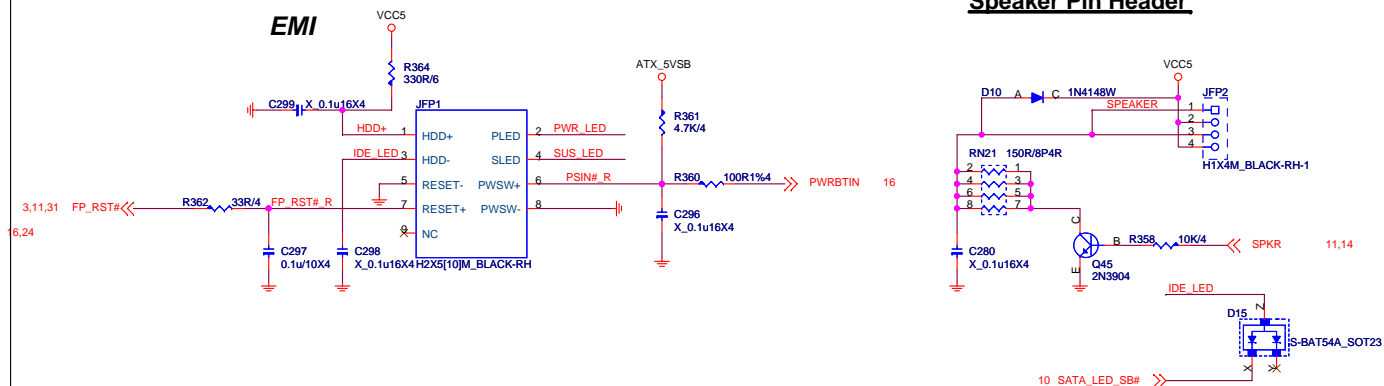
## LED ( for NV5533)



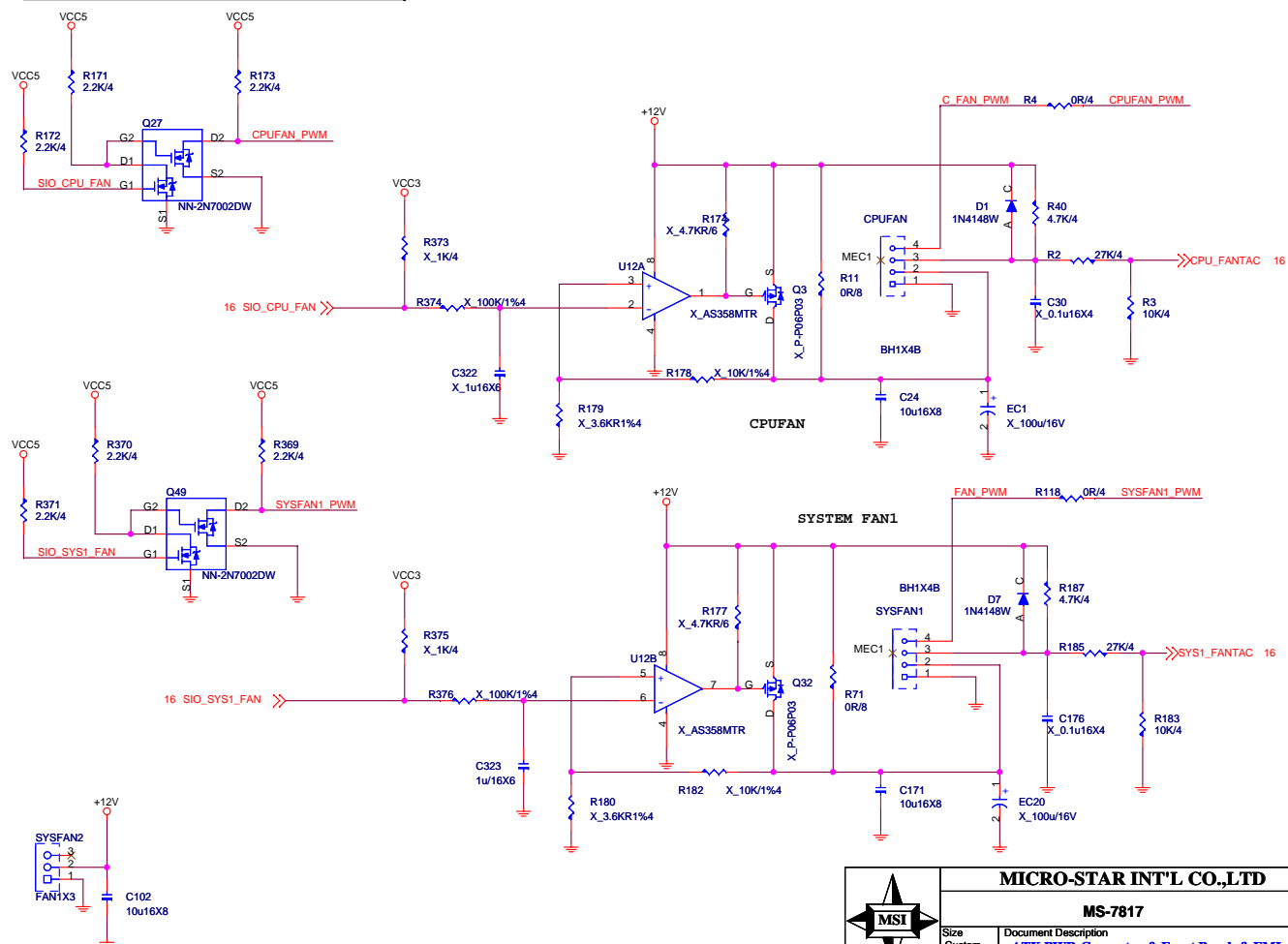
## TPM/JLPC



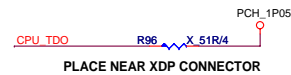
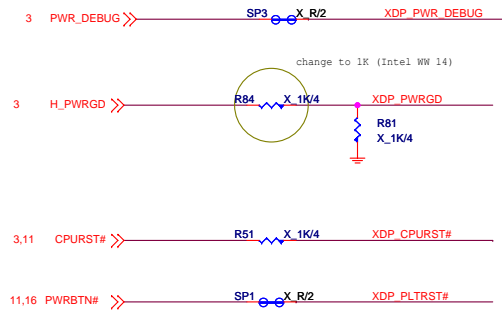
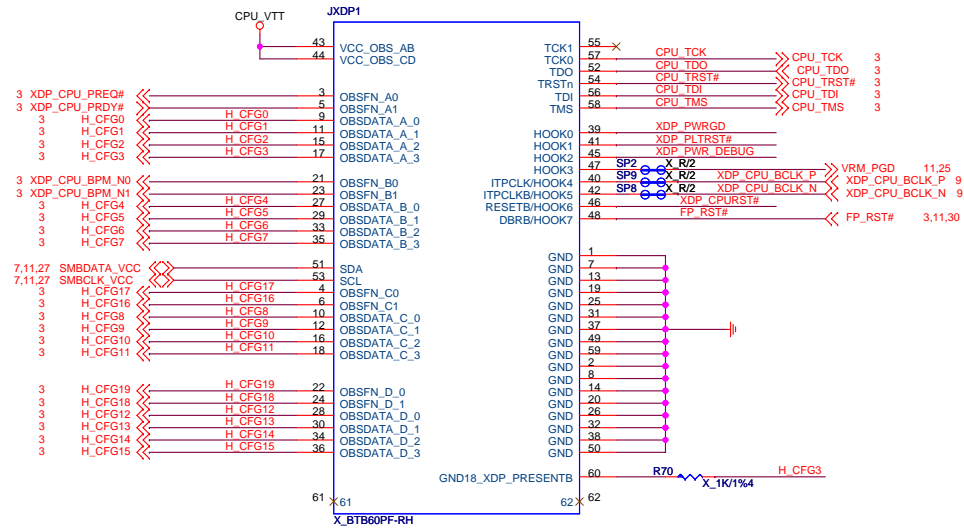
## FRONT PANNEL



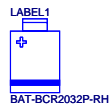
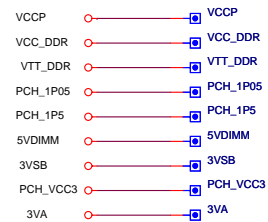
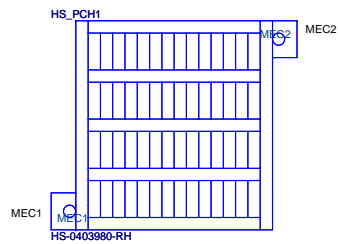
## FAN-COUNT CIRCUIT



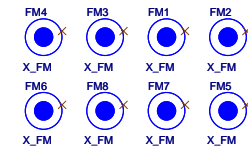
## Reserve debug port 5020



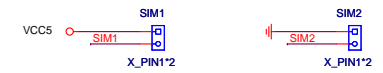
**PCH XDP PWRGD/RESET**



**Optical Fiducial Marks-120**



**Simulation**



**Mounting Holes**

